

ALMA Digital Front-End: Configuration Study.

Final Report

Version 2.0

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Abstract

This report contains an analysis and trade-off study of an ALMA Digital Front-End (DFE) system which includes the digitizers and digital processing in the ALMA receiver cabin, and the digital transport system between the antennas and the centrally located correlator. A revised set of ALMA front-end requirements are proposed. The trade-off between different digitization and signal processing architectures is discussed in the context of a projection of relevant technology development over the next decade. DFE functions are described, including coarse frequency channelization, baseline ripple correction, digital image sideband leakage correction, spurious signal suppression, and delay tracking. The extensibility of the design and digital data transport from antennas is considered. The interface with correlators using both the FX and XF topologies are discussed, noting that a distributed FX correlator performing the first stage of frequency channelization at the antenna dovetails well with the Digital Front-End requirements. The study includes a financial trade-off.

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1 Introduction

Vigorous and transformative investigation of the millimeter/submillimeter sky at high sensitivity and high resolution has benefited from the recent completion in 2013 of the Atacama Large Millimeter/submillimeter Array (ALMA)¹, an effort of 22 countries. ALMA, a versatile interferometric observatory at 5000m elevation in the Atacama Desert of northern Chile, comprises sixty-six precision telescopes which may be arrayed over a 16 km extent on the high Chajnantor plain [1]. Owing to its large collecting area of approximately 6600 m² and its spectral grasp of 8 GHz of spectrum in dual polarizations within the 84-950 GHz range, ALMA provides astronomers with vastly improved spectroscopic sensitivity. Spatial resolutions of 20 milliarcsec were demonstrated recently, revealing a 1 au dark annulus in the TW Hya disk. Using ALMA's excellent imaging quality, dark substructure was found in the galaxy gravitationally lensing SDP.81.

From its conception it was realized that a program of upgrades would be necessary to keep ALMA at the forefront of technology during its projected 30-year operational lifetime. This process kicked-off even before the ALMA inauguration with projects launched to add capabilities that, due to funding constraints, were descope during the construction phase, such as the band 1 receiver covering 35-50 GHz and a phasing capability that enables ALMA to take part in global Very Long Baseline Interferometry (VLBI) arrays. This process will continue with the addition of band 2 receivers which will complete the originally envisaged frequency coverage from 35-950 GHz and with a new study for the next ALMA correlator providing very high frequency resolution, and versatility² several upgrade studies to increase the frequency resolution and bandwidth of digital system and proposals under discussion to add band 2 which will complete the originally envisaged frequency coverage from 35-950 GHz.

Given that the work to complete ALMA would soon be done, attention turned to the question of how best to use the available ALMA upgrade development funds in order to further extend its scientific capabilities in the period up to 2030. To this end the ALMA Science Advisory Committee (ASAC) set up a group to establish a set of scientific priorities for ALMA in the next decade. Their report was further elaborated and combined with a survey of technology status by a cross-disciplinary working group which culminated the release of the ALMA 2030 Roadmap document (see next section).

The "ALMA Digital Front-End: Configuration Study" was proposed as part of the ESO ALMA technology study program and established a Digital Front-end Working Group (DFWG) comprising experts from institutes representing all ALMA regions, including NRAO, JAO, ESO, NAOJ, NOVA/Kapteyn astronomical, University of Chile, Bordeaux University, MPIfR and Harvard Smithsonian. The goal of this work is to identify and evaluate options for optimizing the front-end – back-end architecture using modern digital signal processing techniques. The systems under study would provide the core functions of digitization of the IF band, pass band equalization, fine delay tracking, initial frequency channelization and data transfer to the ALMA correlator. Such a digital processing system could also provide functions such as digital phase and amplitude balance calibration for sideband separating receivers; flexible selection of spectral windows, potentially from different bands or multipixel arrays; removal of polarization leakage terms.

This Final Study report discusses ALMA scientific and technical requirements for ALMA system in the context of the improvements a digital FE processing system could provide. An analysis of the impact of improved calibration accuracy on ALMA observations is presented. The report presents a survey of technologies and trends which can be used in the time span of 10 years (mid term) to create DFE system. Finally, a trade off between several architectures is presented, including a discussion of interface options with different correlator architectures, and a possible technical development roadmap is proposed.

2 ALMA next generation scientific goals and requirements

ALMA is currently the most sensitive millimeter/submillimeter observatory in operation, and has yielded over 1000 publications in its first five years of operation. However, without upgrades ALMA

¹ALMA is a partnership of ESO (representing its member states), NSF (USA) and NINS (Japan), together with NRC (Canada), NSC and ASIAA (Taiwan), and KASI (Republic of Korea), in cooperation with the Republic of Chile. The Joint ALMA Observatory is operated by ESO, AUI/NRAO and NAOJ.

²The approved correlator upgrade to increase the frequency resolution by a factor of 8 has recently been terminated.

runs the risk of not maintaining its position of field dominance. To this end an ALMA Development Working Group (J. Carpenter, D. Iono, L. Testi, N. Whyborn, A. Wootten, and N. Evans; hereafter ADWG) was formed and charged with proposing a science driven vision for ALMA development over the medium to long term (5-15 years) that was prioritized and consistent with the anticipated development budget. The ADWG developed an ALMA Development Roadmap that was approved by the ALMA Board in November 2017, and published as public ALMA Memo No. 612 [2].

The ADWG proposed the following fundamental science drivers for ALMA over the next decade:

Origins of Galaxies

Trace the cosmic evolution of key elements from the first galaxies ($z > 10$) through the peak of star formation ($z = 2-4$) by detecting their cooling lines, both atomic ([CII], [OIII]) and molecular (CO), and dust continuum, at a rate of 1-2 galaxies per hour.

Origins of Chemical Complexity

Trace the evolution from simple to complex organic molecules through the process of star and planet formation down to solar system scales ($\sim 10-100$ au) by performing full-band frequency scans at a rate of 2-4 protostars per day.

Origins of Planets

Image protoplanetary disks in nearby (150 pc) star formation regions to resolve the Earth forming zone (~ 1 au) in the dust continuum at wavelengths shorter than 1mm, enabling detection of the tidal gaps and inner holes created by planets undergoing formation.

Achieving these ambitious goals is currently impossible even with the outstanding capabilities of the current ALMA array; they require maintaining or increase in line sensitivity in addition to bandwidth broadening and increasing the number of spectral channels available. Therefore, the ADWG recommended that the top development priority, based on scientific merit and technical feasibility, is broadening the ALMA receiver IF bandwidth by at least a factor two while maintaining sensitivity; and to upgrade the associated electronics and correlator to: provide more spectral channels, eliminate the aliasing gaps, and reduce the loss due to quantization. The ADWG also recommended improving the scientific functionality of the ALMA Science Archive and supported the study of a range of future upgrade options that it considered fell outside the scope of the period up to 2030.

The new science goals can be achieved with the upgrades proposed in The ALMA Development Roadmap, upgrades that would make ALMA even more powerful and keep it at the forefront of astronomy by continuing to produce transformational science and enabling fundamental advances in our understanding of the universe for the decades to come.

The ALMA Digital Front-end Working Group (DFWG) work directly addresses a key part of the Roadmap primary development recommendation by identifying suitable upgrade options for more than doubling the digitized IF bandwidth at increased bit depth. Additionally, techniques such as digital sideband separation are effective ways to improve ALMA's capabilities as we discuss below. A suitably designed flexible Digital Front-End (DFE) could support future upgrades such as multibeam receivers or dual-frequency operation if those are prioritized beyond the 2030 timeframe considered in the Roadmap.

In order to guide the priorities of the DFWG, we consider the types of observations requested for Cycle 6 (private communication). Of the 1870 proposals received, 351 required mosaics (19%), most of which are on Nyquist sampled hexagonally-packed arrays of pointings. 578 Cycle 6 proposals (31%) requested observations requiring more than one frequency tuning, of which 230 only requested multiple tunings in the same band, and 428 requested tunings in 2 or more different bands. Since all ALMA observations would benefit from improved sensitivity, **we consider the DFE potential impact on sensitivity to be the highest priority for the DFWG.**

There is a consensus that to achieve these goals several ALMA system improvements are needed where this study can have significant impact:

- **Significantly improve instantaneous bandwidth and bandwidth coverage** which requires to at least double up to perhaps quadruple the instantaneous digitization bandwidth from the current 4 GHz per sideband (8 GHz per polarization) to 8 GHz per sideband or more by utilizing possible modular expansion approach.
- **Improving sensitivity** by increasing digitization bit depth to 5 ENOB at least, thus allowing to improve current theoretical correlation efficiency of 86% up to 99%.
- **Provide a modular platform for front-end improvements** by utilizing flexible FPGA DSP and a modular architecture (including data transport) to support any future front-end

receiver improvement needs with the least impact on the rest of the system. Modular platform is aimed at providing a cost effective expansion of the capabilities. This is highly desirable in the view of possible new scientific insights which may need update of such capabilities as well as consideration of focal plane arrays capability in long run. At least, this should support later extension of front-end IF bandwidth coverage by installing additional modules with appropriate capabilities which will work together with previous generation. This will provide significant cost savings.

The followings sections will present trade of studies and a roadmap proposal on what will be possible with appropriate development direction in the 10+ years timescale.

3 Digital Front-End specification

3.1 New Requirements

In this section we reflect on ALMA technical requirements in 10+ years perspective, which are the most relevant for the DFE study.

Table 1 lists the key requirements that the DFWG considers should be modified and which are consistent with the recommendations of the ALMA 2030 Roadmap. Where applicable the table lists the current requirement and the proposed new requirement.

Table 1: Summary of New Requirements.

Parameters	Old Req #	New Value
Receiver IF bandwidth (per sideband per polarization)	4 GHz (IF 4-8 GHz for 2SB or 4-12 GHz for 1SB and DSB)	At least 8 GHz (IF 4-12 GHz); with a goal of 16 GHz (IF 4-20 GHz)
Continuous IF coverage	Anti-aliasing filters result in the loss of about 125 MHz for each 2 GHz baseband resulting in a total usable instantaneous bandwidth of ~7.5 GHz	The processed IF bandwidth shall cover at least a 3:1 frequency ratio with no gaps or lost coverage at the IF band edges
Front-end Sideband Rejection Ratio	>10 dB for 90% of the IF range (SSB and 2SB) >7 dB over 100% of the IF range (SSB and 2SB)	>20 dB with a goal of >30 dB under all conditions
Digital Base band calibration	Analogue equalization only, limited to 2 GHz sub-bands	True digital base band correction with 10 MHz channel spacing *
Correlator bit depth and transport	2 and 3	full 4 bits for all frequency resolution modes/ full IF band
Analogue inputs	2 polarisations, 2 sidebands, 10 frequency bands	2 x 2 x 10 with the possibility to extend
Digital Processing channels	2-pols x 4 basebands	2-pols basebands
Compatibility		DFE concept should be able to support operations with current ALMA XF correlator, ALMA compact array FX correlator, possible future FFX correlator upgrade by adapting FPGA software only.
Flexibility		Where practical the design shall support upgrades to increase the number of IF channels and/or increased IF bandwidth and/or multiplexing.

* In current ALMA ACA (compact array) as well as main correlator has already implemented similar procedure where the channelized scalings applied in the correlator before re-quantizations (BLC FDM modes per 62 MHz sub-band, ACA per-channel after FFT). These have similarities to aspects of what is proposed, although they only work with 3-bit sampled input rather than proposed 5..6.

3.1.1 ALMA Provisional Band-Dependent Performance Requirements.

The provisional requirements that are proposed to be enforced for new cartridge designs from now until the science requirements are updated in 2019 are shown in table 2. This table represents the minimum upgrade necessary to be consistent with the 2030 Roadmap but does not include additional improvements which are expected to be technically feasible within the 2030 scope. The ALMA DFE specifications and architecture should at least support these IF bandwidths but

should aim to be flexible enough to support the goal IF range listed in Table 1, should front-end and correlator technology make those feasible.

Band No.	Freq. Range, GHz	Max. Rcvr. Temp., K (100% of band)	Max. Rcvr. Temp.,K (80% of band)	BW per polarization in IF range, GHz	Front-End Type	IF Range, GHz ^f
1	35–50	32	25	8, HFET	USB	4–12
2	67–95	47	30	16, HFET	2SB	4–12
3	84–116	60 ^a	37 ^a	16, SIS	2SB	4–12
4	125–163	82	51	16, SIS	2SB	4–12
5	163–211	105	65	16, SIS	2SB	4–12
6	211–275	136	83	16, SIS	2SB	4–12
7	275–373	219 ^b	147	16, SIS	2SB	4–12 ^e
8	385–500	292	196	16, SIS	2SB	4–12 ^e
9	602–720	261 ^c	175 ^c	16, SIS	2SB	4–12 ^e
10	787–950	344 ^c	230 ^{c d}	8, SIS	DSB	4–12 ^e

Table 2: Band-Dependent Requirements.

Notes:

^a Noise temperature requirement shown reverted to original version.

^b Relaxed noise temperature, <300 K, for the RF frequency range 370 – 373 GHz.

This relaxation would likely be removed for a future design

^c DSB noise temperature. Future band 9 and 10 designs would likely be 2SB.

^d 230 K over 80% of a reduced frequency range (787-905 GHz).

^e There is interest to increase the IF bandwidth, but the details are not yet decided.

^f At least 3:1 frequency ratio, nominally 4.0 – 12.0 GHz +/- 5.0%

3.2 ALMA requirements

In this section we propose the ALMA front-end/back-end/correlator requirements relevant for the near-term. Achieving or improving upon these requirements should be feasible with the proposed DFE system architecture and for this document these are considered as **Minimum system requirements**. These include specifications from the ALMA front-end including bandwidth upgrade, and rationale for few key specification, such as required dynamic range, required full equivalent number of bits (ENOB) of digitizer (SINAD and white noise).

3.2.1 Critical Technical Requirements.

Table 3 shows technical requirements relevant for the digital front-end – back-end study. These are based on the recommendations in the ALMA Development Roadmap [2] and other inputs. The requirement identification code (# column) indicates to which array the requirement is applicable: "M" refers to the EU (European) and NA (North American) Antennas and/or to the 64-Antennas Correlator.

"T" refers to the Mitsubishi 12 m (PM) antennas or any other 12 m antenna used in the Total Power (TP) antenna array.

"7" refers to the Atacama Compact Array (ACA) 7 m antennas and correlator.

"T/7" refers to the ACA Correlator and both TP and 7 m arrays.

A blank code indicates that the requirement applies to all arrays.

The abbreviations "R", "T" and "T*" in parentheses in the parameter column specify the verification method to be used (see ALMA Project Documentation Standards, ALMA-80.02.00.00-003-G-STD).

Table 3: Summary Table of Critical Technical Requirements.

Parameter	Req #	#	Proposed Value	Sci #
Signal Dynamic range (T*)	227.1		The system shall be designed to accommodate variations in the total power signal level of 4 dB during an observation while meeting the quantization noise requirement #521	
	227.2		The system shall be designed to accommodate an increase in the total power signal level of up to 12 dB during an observation with no more than 25% loss in sensitivity	
	227.3		The system shall have at least 16 dB of gain adjustment to compensate for differences of in IF power level between bands, different hardware (serial numbers), and at different FE tunings	
1st Mixer Sideband Ratio (T)	231		> 20 dB suppression over 100% of the IF frequency range, SSB and 2SB (with a goal of > 30 dB) < 3 dB difference across 80% of the combined IF and LO frequency ranges, DSB	
Front-End: IF output (R)	234		All 2SB FE systems shall output to the BE both sidebands simultaneously	
Freq range, 1st IF (T*)	240		The processed IF bandwidth shall cover at least a 3:1 frequency ratio, nominally 4.0 – 12.0 GHz \pm 5%, with no gaps or lost coverage at the IF band edges	
Total Instantaneous Bandwidth (T*)	250		> 16 GHz \pm 5% per polarization (2SB) > 8 GHz \pm 5% per polarization (SSB & DSB)	
Gain Stability: .05-100 sec (T*)	261		Allan Standard Deviation (ASD) < $1.0 * 10^{-3}$ on time scales of 0.05 to 100 seconds; applies to all antennas	300
Gain Stability: 100 to 300 seconds (T*)	262		ASD < $3.0 * 10^{-3}$ on time scales of 100 to 300 seconds; applies to all antennas	300
Total Power Gain Stability (T*)	263	T	ASD < $4.0 * 10^{-4}$ at time scales of 0.05 to 1.0 sec for the 4 antennas used for total power observations	305
Polarization: Complex gain Stability (T)	264		a) < 0.01 in amplitude and b) < 0.4 degrees of phase for ASD time periods 0.05 to 300 sec	320
Baseband filter: stop-band response (T*)	270		Deleted, replaced by new requirement #280	
Baseband filter: pass-band response (T*)	271		Deleted, replaced by new requirement #280	
Bandpass Shape: gain v.s. freq; wide band (T)	272		Gain variation (p-p) across the whole IF band, due to all system components, under any tuning shall be less than 10 dB	
Bandpass Stability: spectral gain v.s. time (T)	273.1		1 sec: Temporal change in bandpass gain or shape of auto correlation. < -40 dB over 1 second	70
Bandpass Stability: spectral gain v.s. time (T)	273.2		1 hr: Temporal change in bandpass gain or shape of cross correlation < -30 dB over 3600 seconds	70
System spurious responses (T*)	280		Spurious responses in the IF processing system shall be suppressed by at least 40 dB with respect to the wanted in-band response	70

Table 3: Summary Table of Critical Technical Requirements.

Parameter	Req #	#	Proposed Value	Sci #
Broad-band Spurious Signal – Incoherent among antennas (T)	292		a) IF power in incoherent spurious signals shall be < -10 dB per unit bandwidth relative to the nominal system noise power per unit bandwidth. b) stability of the incoherent spurious signals shall be < -20 dB per unit bandwidth relative to the nominal system noise power per unit bandwidth.	
Broad-band Spurious Signal – Coherent among antennas (T)	293		< -17 dB averaged over the continuum bandwidth, before suppression by LO offsetting or phase switching; In those cases where spur suppression is not effective, the requirement is < -47 dB	80
Narrow-band Spurious Signal – Coherent among all antennas (T)	295.1		< -28 dB before interferometric spur suppression (spur signal power relative to the system noise power in a 1 MHz bandwidth) In those cases where spur suppression is not effective, the requirement is < -58 dB	70
Narrow-band Spurious Signal – Spur amplitude stability – Incoherent or coherent among antennas (T)	295.2		< -32 dB rms of a random component, and < - 56 dB constant difference component (the difference of the spur signal power in two switching states, relative to the system noise power, both in a 1 MHz bandwidth)	70
Spurious Signal: Stability of spur amplitude integrated over 2GHz bandwidth of Total Power Detector (T)	297		< -48 dB rms of a random component, and < -72 dB constant difference component (the difference in two switching states of the aggregate spur signal power over the 2 GHz baseband, relative to the system noise power)	70, 80
Digital Signal Transmission (T)	311		The cable delay in each DTS should remain constant within ± 8 ns for at least 2 weeks.	
Digital Signal Transmission – Bit Error Rate (T*)	312		The Bit Error Rate (BER) for each DTS should be better than 10 ⁻⁶ .	
Sampling clock: fine delay steps (R)	323		Variable phase for fine delay, < 1/16 sample accuracy.	
Sampling clock: common to all antennas (R)	324		Common to all channels at an antenna.	
Sampling clock: synchronization to correlator (T)	325		Delay changes inserted at both the BE and correlator shall be synchronized to better than 500 μ s.	
Detection and correlation				
Total power detectors (R)	510		Total power detectors shall be provided for each IF channel for engineering monitoring and science purposes	
Total power detectors: frequency range (R)	510.1		The engineering detectors shall cover the complete IF range (requirement 240)	

Table 3: Summary Table of Critical Technical Requirements.

Parameter	Req #	#	Proposed Value	Sci #
	510.2		The science detectors upper and lower frequency range shall be configurable in increments of 0.1 GHz or less within the IF range (#240)	
Total power detectors: accuracy (T*)	511		Accuracy 1% of full scale (after linearity correction) and shall meet the stability requirements #261 – #263	
Total power detectors: Full scale	511.1		The total power detectors full scale IF power level shall be +13 dB relative to the nominal sky power level	
Total power detectors: sampling interval (R)	512		Sampling interval for science detectors shall be configurable over the range 0.5 msec to 10 s at > 99 % efficiency	
Total power detectors: Dynamic range	513		The total power detectors shall have a dynamic range > 13 dB	
Quantization resolution (R)	521		The loss of sensitivity at any frequency on the IF passband due to quantization and digital processing in the signal chain shall be less than 4% for all conditions of passband power variation (gain flatness) and allowed input signal level changes	190
System Restart: calibration (T)	618		It shall be possible to perform warm restart (soft resets) or power cycles of equipment at the module, sub-system and system level, including the Full System Restart, without recalibrating the telescope beyond those calibrations carried out during normal observation activities.	
System Restart: time (T)	619		It shall be possible to restart any part of the system, including the full system (supposing all receivers are operational i.e. at nominal cooled temperature), in less than 15 minutes	
WVR: Correction error & rate (T)	622	M	Path length correction error (rms) $\delta L < (0.01w + 10) \mu\text{m}$, with a sampling rate < 1 Hz.	290

In the following subsections the most critical requirements, requiring a trade-off will be discussed.

3.2.1.1 Signal Dynamic Range, Passband IF variation and Quantization Efficiency

There are three critical parameters that drive the required ENOB versus sample-rate trade-off in the selection of samplers and the choice of IF architecture, these are: Signal Dynamic Range, Passband IF variation and Quantization Efficiency. These are dealt with in the following subsections.

Signal Dynamic Range

This is the range of signal power levels that the IF chain has to cope with and can be broken down to two parts:

- Power level changes during the observing sequence, for example due to sky opacity changes from weather or changes in elevation, and gain drift in the receiver system.
- Power level changes that occur from observation to observation (e.g. due to LO1 changes), from band to band, and from front-end to front-end.

The first part always has to be accommodated by the ADC regardless of architecture in order to keep the analog IF signal processing path to be unchanged during the complete duration of

a calibration and science target observation sequence. This is because any practical circuit for modifying the overall gain of the IF system will introduce a frequency dependent change in the complex gain of the system thus giving rise to both phase and amplitude calibration errors.

However, the variations from the second part can be accommodated by adjusting the IF system gain immediately prior to starting the calibration at a new frequency or configuration thus reducing the dynamic range that the samplers need to cope with.

Table 4 gives the sources of power level changes during an observation for three cases: non-solar science target observing, atmosphere calibration sequence, solar observing. It is not considered feasible to compensate for these variations in power level by using adjustable attenuators or gain elements in the IF system in front of the samplers.

Source	Dynamic range	Required quantization efficiency	Notes
Sky brightness changes IF level setting error	3 dB 1 dB	96% 96%	Neil Phillips (private communication). Combination of IF attenuator resolution and setting error.
Sub-total: science targets	4 dB	96%	System Requirements #227.1 & #521
AtmCal calibration sequence IF level setting error	12 dB 1 dB	75% 75%	Hot load versus cold sky (see Table 7 for the band dependent values). Combination of IF attenuator resolution and setting error.
Sub-total: flux calibration	13 dB	75%	System Requirement #227.2
Solar observations IF level setting error	12 dB 1 dB	90% 90%	TBC Receiver detuning or optical attenuator. Combination of IF attenuator resolution and setting error.
Sub-total: solar observing	11 dB	75%	Provisional value, TBC.

Table 4: IF power level dynamic range and quantization efficiency requirements during an observation. The first part of the table applies while observing the science targets (except the Sun); the second part applies during the atmospheric and flux calibration cycle; and the third part applies during solar observations.

Table 5 gives the power level changes between observations. These changes may be compensated with an adjustable attenuator in the IF system before the sampler, i.e. to reduce the range of signal levels the sampler has to operate with. If an adjustable attenuator is **not** used to compensate for these level changes, then the sampler has to accommodate these changes in addition to those listed in Table 4 with the stated minimum quantization efficiency applicable to each case.

Source	Dynamic range	Required quantization efficiency	Notes
Cartridge variation	16 dB	96%	System Requirement #227.3.

Table 5: IF power level changes between observations. These level changes arise due to differences in net signal gain between different LO tunings for the same receiver, between different receivers of the same band and between different receiver bands.

Passband IF variation

This is the signal level variation across the passband due to ripple, gain-slopes etc. The relevant bandwidth for this discussion is that which pertains to the sampler baseband input. The proposed requirements are listed in Table 6.

Quantization Efficiency

The relatively coarse quantization employed by samplers typically used for radio astronomy intro-

Case	Value	Notes
Gain variation across whole IF band	13 dB	Unchanged (#272)
Gain variation across baseband	8 dB	Based on the existing requirement of 8 dB across 2 GHz (#271)

Table 6: IF level variations allowed across the IF passband. The first applies to variations allowed across the whole of the IF band. The second applies to variations which occur within the baseband of the ADC (this only applies to architectures that split the IF band into multiple bands each feeding an ADC).

duces errors in the representation of the incoming signal that can be viewed as additional noise. Quantization efficiency is the relative loss in signal-to-noise ratio resulting from the introduction of this noise in the quantization process. This leads to the concept of quantization efficiency. For the analysis that follows quantization noise is defined as $1 - \text{quantization efficiency}$. The level of this quantization efficiency and therefore noise relative to the wanted signal depends on the number of sampler levels and the signal level relative to the sampler level spacing. Quantization efficiency is discussed in detail in Section 4.1.1.

For the quasi-random signals with a Gaussian distribution being digitised in ALMA, the quantization noise is spread uniformly across the Nyquist band. This implies that the signal to noise ratio across the baseband is proportional to the variation in signal level across the passband at the sampler input. This implies that the signal to quantization noise ratio in troughs of the passband signal level is degraded by the depth relative to the average power density or, typically, half of the peak to peak variation across the baseband passband: 8 dB peak to peak variation degrade the SNR by 4 dB.

3.2.1.2 ALMA amplitude calibration sequence

Part of the standard calibration sequence for ALMA observations measures the power levels detected while looking at the sky, an ambient temperature black-body load (typically at 16 C) and a heated black-body load at a temperature of 85 C. The IF power level is first set to the level that maximizes sensitivity while observing the science target. Thereafter the receiver looks at the ambient and hot loads. The resulting changes in signal level during this cycle depend on the effective sky temperature, the opacity, the receiver noise temperature and the temperatures of the two calibration loads.

Table 7 shows the measured values of receiver and system noise temperatures at the 10th percentile, and the dynamic range between observing the hot load and cold sky at the 90th percentile, for bands 3 – 10 (the values for bands 1 & 2 are projected values based on expected receiver performance and sky transmission). This shows that IF level changes of up to slightly more than 10dB may be expected during the calibration sequence.

Band #	Trec /K	Tsys /K	Dynamic range /dB
1	25	37	10.2
2	30	45	9.3
3	30	50	8.9
4	33	53	8.7
5	28	63	7.9
6	34	66	7.7
7	50	107	5.8
8	90	260	2.4
9	77	320	1.3
10	158	470	0.4

Table 7: Empirical band dependent receiver noise temperature and system temperature at the 10th percentile as measured in 2017 & 2018. (Bands 1 & 2 are theoretical values). The quoted noise temperatures are SSB values for all bands except 9 & 10 which are DSB values. The fourth column shows the 90th percentile dynamic range required for atmospheric calibration using the standard ALMA calibration loads at temperatures of 358 K & 290 K.

3.2.1.3 Digital correction of phase/amplitude imbalance

Digital correction of phase & amplitude imbalance in 2SB mixers should allow much improved image suppression, especially when high dynamic range digitizers are being employed. Laboratory demonstrations have shown that image rejection ratios up to 50 dB are possible with an 8 ENOBs digitized 2SB system, see Section 4.4.1. The main advantage of sideband separation at DFE is utilizing full noise bandwidth and dynamic range of the digitizer allows to suppress not only lines in the image band, correlated between ALMA antennas, but also sky noise and optical component noise arriving at a single antenna much like the analogue quadrature sideband separating scheme as already employed for ALMA bands 3 through 8. We would like to estimate the impact of the digital sideband suppression system on the system noise temperature level over the existing analogue 2SB ALMA cartridges. The existing analogue sideband ratio is taken to be $SBR = 7$ dB as worst case and $SBR = 12$ dB as typical case. It is recognized that SBR for ALMA cartridges is function of both LO and IF frequency and in many cases may exceed 15 dB for some parts of IF band at given LO frequency, however it is not possible to reach such performance for all IF band and all LO frequencies for existing ALMA 2SB cartridges.

Let us consider the measured ALMA front-end noise temperature T_{SSB} distribution as shown in figure 1 as black line. expressed in DSB noise temperature. The T_{SSB} for ALMA band 9,10 is obtained by doubling the DSB values. In order to investigate trend of the noise temperature we build the noise model of the system. First we estimate the SIS mixers SSB noise temperature

$$T_{SSB,mix} = 2 \left(\frac{T_{IF} * f}{400 * 10^9} + 2 * \frac{hf}{2k} \right), \quad (1)$$

where f is signal frequency; h and k Planck and Boltzmann constants respectively, $\frac{hf}{2k}$ is photon energy with quantum noise is taken as double value, $\frac{400*10^9}{f}$ represents model of SIS mixer gain, while IF system noise temperature T_{IF} is taken as 10 K. The calculated $T_{SSB,mix}$ is shown in figure 2 in dashed line labeled "Mixer model" (orange color). This line clearly describes the trend in measured T_{SSB} for band 5-9 and for bands 5-7 it also describes the trend of noise temperature within the band, indicating that these bands are already close to intrinsic limit of the mixer noise. For the top part of band 9 and especially band 10 the deviation is larger and can be attributed to increased losses in superconducting materials at these frequency. Notably, bands 2-4 depart significantly from general model trend as if there is a fixed noise contribution on top of $T_{SSB,mix}$. This fixed contribution can be explained by an increased noise coming from warm optics, which only exists in band 1-4 in ALMA system. When this optics contribution T_{opt} is included, we can create final model for T_{SSB} :

$$T_{SSB,model} = T_{SSB,mix} + T_{opt}, \quad (2)$$

where $T_{SSB,mix}$ is given by (1) and T_{opt} has been estimated from the fit to a measured T_{SSB} . A simple estimate for T_{opt} of a fixed value of 20 K for bands 1-4 and 8 K for bands 5-10 was sufficient to obtain a fit $T_{SSB,model}$ labeled "Trec Noise Model" in the figure 1. The optics contribution T_{opt} is shown in the same figure by dashed line. For higher bands, the optical contribution comes mainly through cryostat window and LO insertion coupler and is small relative to receiver noise temperature, while for lower bands relatively large contribution comes from warm optics elements and their spill-over.

Finally, if we know the approximation of optical part of noise temperature T_{opt} we can calculate intrinsic underlying mixer DSB noise temperature $T_{DSB,mix}$, which together with sideband ratio $SBR = 7$ dB or $SBR = 12$ dB results in measured noise temperature according to the following equation:

$$T_{DSB,mix} = 0.5 \left(T_{SSB} - T_{opt} \left(1 + \frac{1}{SBR} \right) \right). \quad (3)$$

Calculated $T_{DSB,mix}$ is shown in figure 1 with label "Derived DSB mixer noise" and it only depends on assumption of T_{opt} , sideband ratio SBR and measured T_{SSB} . Calculated values closely follow the quantum limit, shown in the same figure for reference, for lower frequencies and slightly departs from it above 400 GHz.

Now it is possible to vary SBR and calculate its impact for front-end noise temperature $T_{rec,model}$ using following equation:

$$T_{rec,model} = 2 * T_{DSB,mix} + T_{opt} \left(1 + \frac{1}{SBR} \right). \quad (4)$$

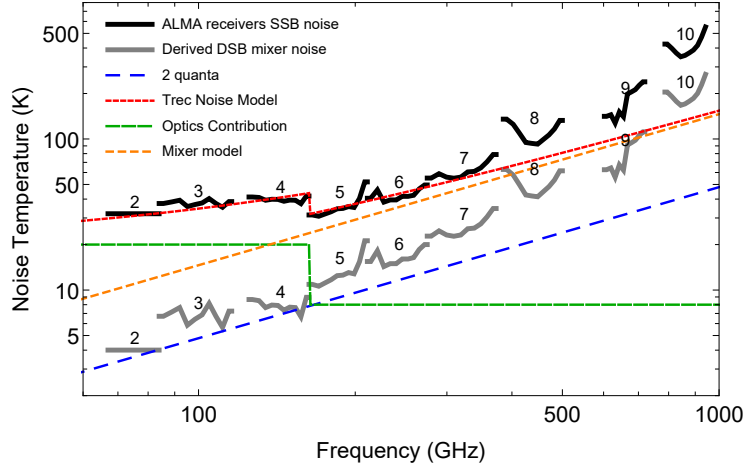


Figure 1: Model results describing measured performance of ALMA front end receiving system. See explanation in text

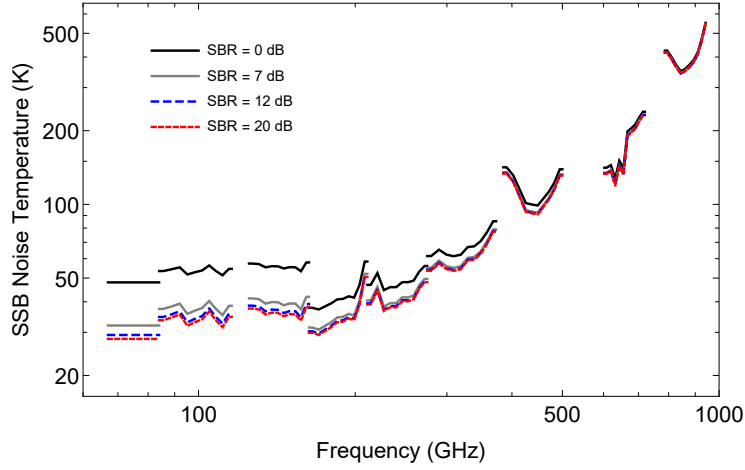


Figure 2: Front-end receiver noise temperature estimated for different sideband ratios SBR

Estimate for $T_{rec,model}$ are shown in figure 2. The $SBR = 0$ dB curve corresponds virtual DSB case and is only applicable to ALMA band 9,10 in current system. The $SBR = 7$ dB replicates measured T_{SSB} by definition of model set up. Finally, $SBR = 20$ dB presents receiver noise with a digital sideband separation of 20 dB. Significant relative noise change can be stated for low frequency bands 2-4, while the influence of SBR diminishes at higher frequency bands. Since observing efficiency is proportional to T_{noise}^2 one can already estimate impact of as large as 25 % in integration times for lower frequency bands relative to $SBR = 7$ dB and 12 % relative to $SBR = 12$ dB.

For estimating full impact the developed model is used together with atmospheric data for zenith brightness T_a and zenith opacity α_a for 25th percentile in ALMA site. The resulting system noise temperature $T_{SSB,sys}$ including optics and atmosphere can be calculated using the following equation:

$$T_{SSB,sys} = \left(T_{rec,model} + T_a \left(1 + \frac{1}{SBR} \right) \right) / \alpha_a / 0.8, \quad (5)$$

where we assume that aperture efficiency of the system is 0.8 and system spill-over is coupled to cold sky. The resulting estimates are present in figure 3. Here again $SBR = 0$ dB corresponds to DSB mixers in ALMA band 9,10. Significant gain in system noise temperature for $SBR = 20$ dB relative to $SBR = 12$ dB (current system) now can be observed both for low frequencies due to relatively large optical contribution and for high frequencies due to relatively small atmospheric transmission and large zenith atmospheric brightness. The observing efficiency gain vs SBR is presented in figure 4 and expressed as decrease of observing time relative to current $SBR = 12$ dB

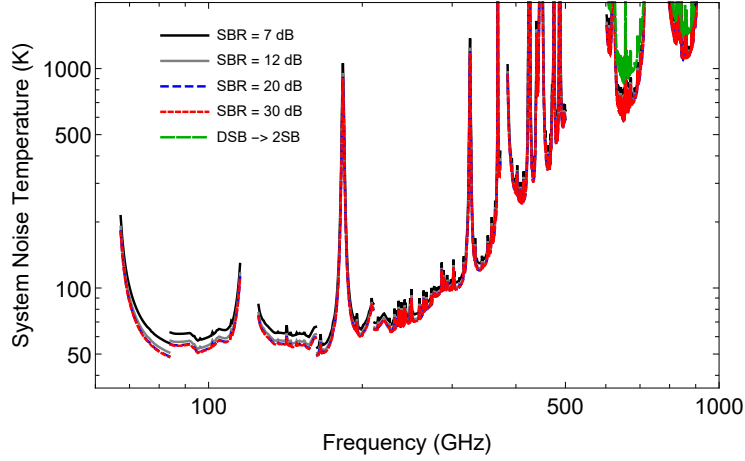


Figure 3: Calculated SSB system noise temperature $T_{SSB,sys}$ for 25th percentile atmospheric conditions at the ALMA site and different sideband ratios SBR

system and worst case $SBR = 7$ dB system.

Observing time gain of more than 5..10 % can be obtained for all bands, with maximum up to 40 % for band 2-3. ALMA band 1 is not considered throughout the modeling as this is pure SSB system, which can not be improved digitally. Relative gain of implementing 2SB band 9,10 systems is also shown in figure 4 as $SBR = 0$ dB relative to $SBR = 7$ dB, demonstrating gains well above 40 % for spectral line cases, based on noise consideration only. Increasing SBR further than 20 dB does not demonstrate significant gain in observing time by the above model.

The data in figures 3 and 4 is based on a moving average of sky transmission/brightness with a window size of approximately 1 GHz window in frequency. This masks another aspect to be considered: the presence of strong telluric lines in the image sideband. These lines are not correlated between antennas and their effect on T_{sys} can not be suppressed in the correlator by LO switching. The telluric lines can produce antenna temperatures up to 200K so image suppression of 20dB is needed to keep their contribution to T_{sys} below 5% in the lower bands and ideally it should be > 25 dB.

The following items listed below are noted here for completeness, they are discussed in more detail in Section 4.4.1 of this document:

- Time overhead to calibrate out imbalance needs to be considered: it has been demonstrated that proposed system has enough resources to do that with margin

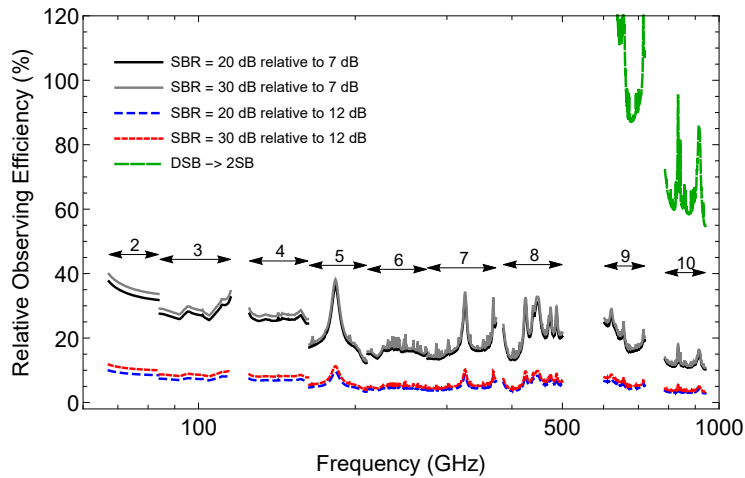


Figure 4: Calculated integration time gain for 25th percentile atmospheric conditions at ALMA cite and different sideband ratios SBR . Gain is relative to $SBR = 7$ dB worst case and $SBR = 12$ dB typical case. ALMA band frequency coverage is indicated by arrows and band numbers.

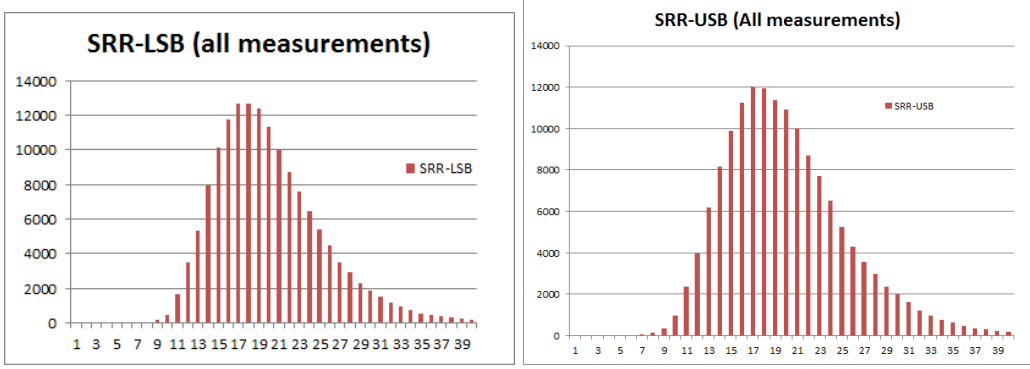


Figure 5: Distribution of sideband rejection ratio data for all Band 5 receivers. Data is taken from qualification measurements.

- How can the correction coefficients be determined? : Coefficients can be determined by calibration using additional weak RF source (like superlattice harmonic mixer, or photo mixer) mounted on robotic arm.
- How stable is the suppression under real-world conditions? : Stability really depends on the required suppression. Levels of $SBR = 20$ dB can be achieved in a pre-calibrated system without re-calibrating for as long as the system is not modified, also going through warm-up/cool down cycles
 - Determines realistic suppression level & calibration interval: additional measurement on ALMA system is required to determine representative ALMA front-end specific timings.

It must be noted, that for simplicity the frequency offset between LSB and USB has been ignored and all relevant values have been calculated at the same signal frequency.

In addition, it is useful to estimate gain in sensitivity (or related observing time) related to improvement due to better image rejection of digital calibration system using real SBR data. Figure 5 shows distribution of sideband rejection data for all Band 5 receivers. The effective average SBR level for this data is about 17 dB. The red curve "SBR=30dB relative to 12dB" from Figure 4 gives relative observational efficiency improvement of about 6% on average. Difference in 5 dB between SBR of 12 dB and 17 dB will correspond to change of this number about 3 times. As result, the improvement in observing time for ALMA due to digital SBR calibration can be estimated as 2%.

In conclusion, increasing the sideband ratio from worst case of 7 dB given by hardware to 20 dB using digital processing, results in solid measurable observing efficiency gains of 15% on average and up to 30% for lower frequency bands. For single-dish, total-power observations a further increase image rejection up to 40 dB is beneficial to suppress ghost spectral responses that can not be suppressed in the correlator. The gain in integration time for typical $SBR = 12$ dB value is somewhat lower but still significant. Alternatively, the ability to use DSP techniques to improve image rejection potentially allows relaxed hardware image rejection to be traded for improved receiver performance, such as T_{rec} , or reduced cost.

3.2.1.4 Continuous IF band coverage for line searches

The ALMA roadmap vision document [2] specifically outlines that it is highly desirable to have continuous, complete coverage of 4 – 12 GHz to make frequency scans more efficient: stepping LO 1 by 8 GHz gives perfect coverage with no overlap or gaps.

Let us consider optimal RF band coverage for a mixer with IF passband spanning from f_{min} to f_{max} . For optimal coverage by stepping LO1 frequencies one requires rational fraction relation between mixer coverage gap of $2f_{min}$ and mixer SSB bandwidth of $f_{max} - f_{min}$. This can be expressed as follows:

$$2f_{min} = (f_{max} - f_{min}) \frac{n}{m}, \quad (6)$$

while ratio of f_{max}/f_{min} takes a form:

$$\frac{f_{max}}{f_{min}} = 2\frac{n}{m} + 1, n = 1, 2, \dots; m = 1, 2, \dots \quad (7)$$

For $m > n$ coverage gap is larger than IF bandwidth, for $m < n$ coverage gap is smaller. Continuous band coverage is for small n, m is illustrated in figure 6.

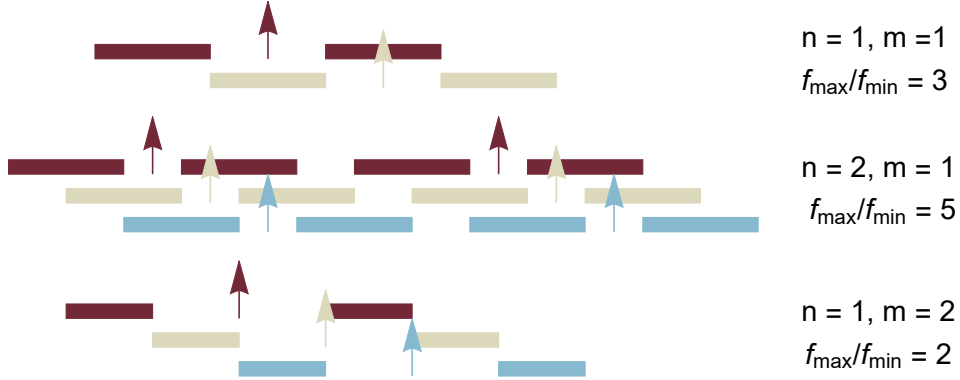


Figure 6: Diagram, illustrating continuous RF band coverage for different n and m from equation (7). It is illustrated, that full ALMA RF band can be covered to achieve uniform level of integration efficiently i.e. by shortest integration time. See further comments in the text.

Case $n = 1, m = 1$ corresponds to the special case $m = n$ and results in $f_{max}/f_{min} = 3$ which is realized in principle for the ALMA DSB mixer bands 9 & 10 (neglecting the gaps caused by the anti-alias filters) and is proposed for the ALMA 2030 upgrade, see Table 2. Continuous band coverage of 32 GHz can be achieved by stepping LO1 only 2 times. Case $n = 1, m = 2$ corresponds to the current ALMA system coverage for 2SB bands 3-8 (neglecting the gaps), covering 4-8 GHz with $f_{max}/f_{min} = 2$, 3 LO1 tunings are needed to achieve continuous RF coverage of 24 GHz with uniform integration time. Another case, which of interest is illustrated by $n = 2, m = 1$ in the figure. It results in a particular large $f_{max}/f_{min} = 5$, which make efficient use of the available digitizer bandwidth in direct digitization options. As seen in the figure, also 3 LO1 steps are needed to achieve continuous uniform integration coverage for most of the band, excluding small part at RF band edges. As in any of the system, IF coverage is extended periodically to cover RF band completely. Amount of steps for continuous coverage n_{step} can readily be calculated using following relation:

$$n_{steps} = n'm' + 1, \quad (8)$$

where n' and m' are minimum integer values satisfying

$$\frac{n'}{m'} = \frac{n}{m} \quad (9)$$

Choosing a more complex n/m fraction increases the number of LO1 steps needed and reduces the integration time needed at any given LO1 frequency. Thus LO1 switching time overhead becomes an important consideration and should be avoided to maximize observing efficiency, assuming that T_{rec} is uniform across the IF band. This overhead in current system is prohibitively large because of need of phase calibration at each switching step.

The current system allows coverage of 3.75 GHz out of (mainly) 4 – 8 GHz IF so 3 tunings are needed to cover the 8 GHz gap between LSB & USB instead of the ideal two. Taking into account that uniform integration time for each subband is desired for further processing, scanning efficiency is decreased by approximately 33% and so will be the gain in implementing frequency plan fulfilling Eqn (7) without increasing total bandwidth. The current system scanning strategy may be re-optimized using a complex n/m fraction closely describing 3.45 GHz out 4-8 GHz band coverage.

Any f_{min} and f_{max} satisfying (7) can be chosen covering any selected IF bandwidth $f_{max} - f_{min}$ where for direct digitization large f_{max}/f_{min} is the most beneficial, while for a system which includes a down-converter before digitization a simple $f_{max}/f_{min} = 3$ can be chosen as it delivers the most efficient RF band coverage with minimum number of LO1 steps.

3.2.2 Design Requirements

General design requirements which would be applicable to the detailed design are shown in table 8 and these may be borne in mind when considering trade-offs in this study.

Table 8: Design requirements.

Parameters	Req #	#	Existing Value	Sci #
3.2.3 Standard parts [FEND-40.00.00.00-00030-00 / R]			Standard, unmodified commercially available components shall be used where possible.	
Use of Line replaceable units (LRUs)			LRUs shall be used where practical.	
7.1 Continuous use [FEND-40.00.00.00-00750-00 / R]			The front-end assembly shall be designed for continuous use.	
7.2 MTBF [FEND-40.00.00.00-00760-00 / A]			The mean time between failures of a front-end assembly shall exceed 11.000 hours.	
7.5 Lifetime [FEND-40.00.00.00-00780-00 / A]			The lifetime of the front-end assembly shall be greater than 15 years.	
Flexibility			Where practical the design shall support upgrades to increase the number of IF channels and / or increased IF bandwidth.	

3.2.3 Interfaces

3.2.3.1 Power

The following table 9 gives the available power and presently used UPS ("clean") power in the antenna cabin. There is probably at least 5 kW of spare capacity.

Table 9: Power requirements.

Item	Allocated Power	Actual power used
Front-end electronics	2 kVA / 1.25 kW	0.4 kVA
Back-end analog rack	2.2 kW	0.5 kW
Back-end digital rack	3.0 kW	0.3 kW

3.2.3.2 Cooling

In general commensurate with the allowed power dissipation and temperature requirements. Cooling in FE electronics assembly is probably marginal.

3.2.3.3 Thermal

Temperature in range: 16 – 22 C

Rate of change of temperature: less than 1 C per hour

3.2.3.4 Mass

The following table 10 gives the mass budget in the antenna cabin. We conclude here that front-end mass can not be increased significantly and that it appears feasible to replace the existing back-end equipment (IF processor, 2nd local oscillators, digitizers etc) with a new digital system.

Table 10: Mass requirements.

Item	Allocated mass	Actual mass
Front-end attached to FE support structure	980 kg	931 kg *
Back-end analog rack	375 kg	185
Back-end digital rack	350 kg	135

*NB The front-end assembly is 20 kg over the allocated budget of 750 kg.

3.2.4 Ancillary Requirements

Ancillary requirements, summarized in table 11, need to be borne in mind but probably do not directly impact the digital FE/BE architecture.

Table 11: Ancillary requirements.

Parameters	Req #	#	Existing Value	Sci #
Independently Tunable subarrays (R)	420	M	It shall be possible to run at least 4 independent arrays (sub-arrays). Each of them can be pointed in different times to different sources and tuned to different frequency.	390
	420	T/7	It shall be possible to run at least 2 independent arrays (sub-arrays). Each of them can be pointed in different times to different sources and tuned to different frequency.	390
Sub-arrays switching time (T)	425		The generation of a sub-array, for a 300s observation, shall not increase the duration of execution of the relevant SB by more than 3% or 1 sigma, whichever larger.	
Frequency tuning: within FE band, time (T)	430		< 1.5 sec for intraband tuning over whole band.	40
Frequency tuning: between FE bands, time (T)	431		< 1.5 sec interband, switching to a FE band in standby mode.	50
Freq Switching: time & range (T)	432		Up to 10Hz rate with a < 10 msec (rise and fall time) (Frequency throw up to of 25 MHz sky frequency; Spectral line total power mode only & within the same FE band)	
FE & LO1: number of bands in standby (R)	433		Up to two bands may be in standby mode while one band is in operational mode, or up to three bands in stand-by mode and none in operational mode.	50
Phase Switching: LO1 180° & 90° (R)	441		180° and 90° phase switching inserted in the 1st LO	
Phase Switching: Settling time (T*)	442		1st LO PLL effective time constant to achieve the desired phase shall be < 1 μ s.	
Phase Switching: Walsh functions (R)	443		Walsh functions, with maximum 128 sequence for 180° series; maximum 128 sequence for 90° series; orthogonal by antenna;	

Table 11: Ancillary requirements.

Parameters	Req #	#	Existing Value	Sci #
Phase Switching: Synchronization (T)	444		Phase Switching synchronization between FLOOG (that applies the switch) and the BE (that removes it) in the same antenna shall be better than 100 ns Switching delay difference, among the 4 IF channels in the BE in each antenna shall be better than 100 ns After the delay correction applied in the Correlator, for antennas receiving the incoming signal in different times, the synchronization shall be better than 100 ns. Sign reversal relative to correlator dump, < 10 μs	
LO Offsetting (T)	446		It shall be possible to offset the LO1, BE down-conversion or correlator from their nominal values by integer increments of 125MHz/212 (30.5176 KHz)	
LO Return to Phase: No phase ambiguity (T)	450		All frequency synthesis unambiguous	
Delay Errors: Time, phase drift (T)	451		< 22 fsec, Allan SD with T = 10 to 300 seconds (drift)	
Delay Errors: Time, phase noise (T)	452		< 65 fsec, RMS about 10 sec average (noise)	290
Delay Errors: Continuous operation (T)	454		System shall typically operate for at least one hour with no step discontinuities in system delay > 10 fsec	
Frequency stability (T*)	460		Allan std dev, frequency < $2e^{-11}$ for T = 20-300 sec.	
VLBI: Array number (R)	461		VLBI Support shall be provided to minimum one Array	380
Correlator output rate: cross-correlation (T)	541.1		16 msec integrations and readout interval, all baselines.	240
Correlator output rate: autocorrelation (T)	541.2		1 msec integrations and readout interval, all antennas	240
Correlator output rate (T)	542		1280M complex correlations per second	
General				
Archive writing rate (T)	610		≥ 600 MB/sec	
Phased array (R)	631		Array shall be usable as a single station (phased up)	370
Real-time phased array (R)	632		Real-time phasing up is required.	370
Phase sub-array possible (R)	633		Sum output available for any subset of antennas.	370

3.3 Progress in performance of front-end designs similar to the current ALMA front-end configuration

In this subsection we give an analysis of progress in performance of front-end designs, similar to the current ALMA front-end configuration. The focus is on gain variation and image rejection. Making this analysis we keep in mind that the current IF bandwidth of ALMA 2SB receivers is only 4 GHz (normally 4-8 GHz IF), but the requirements for new receivers are expected to be at least 8 GHz (4-12 GHz IF), or 12 GHz (4-16 GHz IF), as it is already requested for future ALMA

Band 2 receiver) , or even more.

3.3.1 IF ripple (based on ALMA Band 8 2SB receiver compared with new SIS generation of SIS receivers)

For analysis of IF ripples and gain variations we take as example the new SIS receivers developed recently by NAOJ and compare their performance with the data from cartridges delivered by NAOJ to ALMA, particularly Band 8. We use development of NAOJ group as an example, because (1) it demonstrates one of best progress in SIS receiver technologies (both on receiver and on SIS junction production level), (2) there is access to the data needed to make proper analysis.

3.3.1.1 Band 8 cartridge IF variation in 4 GHz range

Figure 7 shows the IF power spectra and IF gain variation of a typical delivered Band 8 receiver. One can conclude, the gain variation is within 4 dB range, which is with margin within the ALMA specification.

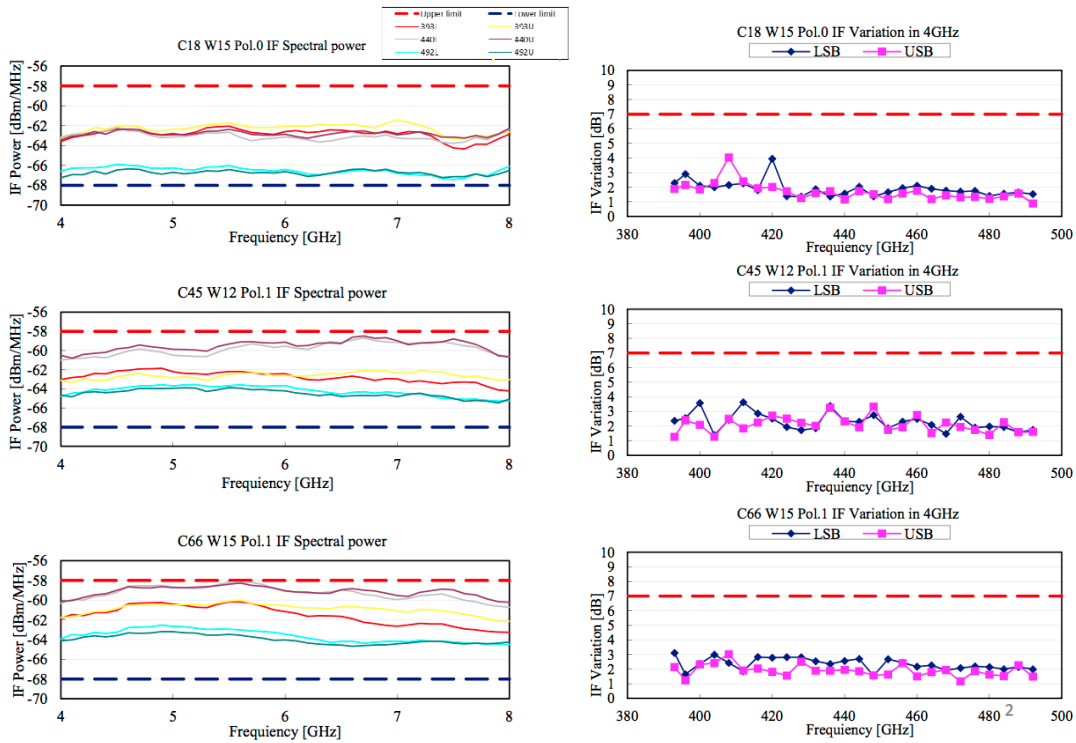


Figure 7: Typical Band 8 cartridge IF spectra (left plots) and gain variations (right plots) in 4 GHz range

3.3.1.2 Receiver IF ripple calculation for two DSB configurations (4-20 GHz)

The latest development at NAOJ in the fields of SIS mixers is presenting receiver Band 7+8 (275-500 GHz) design. $J_c = 40\text{kA/cm}^2$. $R_n = 4.2\Omega$ (PCTJ). $R_{dyn} = a \times R_n$ ($a=8.8-21.3$). This is a promising technology for potential ALMA upgrade, because it can show competitive sensitivity [3], allows combing of two bands in one cartridge and demonstrates extremely wide IF of 4 to 20 GHz.

Two types of IF chain are analyzed (see figure 8). Note that the IF matching circuit of the SIS mixer is optimized for the direct connection with an LNA produced by LNF to maximize performance of the SIS-mixer-amplifier module with respect to noise temperature and the bandwidth. The reflection coefficient at the IF port in the SIS mixer is around 5-10 dB referring to a 50 Ohm load impedance. The LNA performance used in the simulation is equivalent to a typical LNF

4-23 GHz amplifier with reflection coefficients of -7 dB and -10 dB at the input and output, respectively, in the worst case, and gain of 35.5-37.7 dB (see figure 11). The isolator is assumed to have characteristics of -20 dB isolation, perfect reflection coefficient, and no insertion loss. Preliminary simulations for these schemes are shown in the figure 9. This is done to compare these two cases. Clearly, the case with isolator (or with amplifier with low reflection losses) gives much smaller gain variation. From this plot one can expect that gain variations could be kept within 4 to 16 GHz range below 4 dB with isolator and below 7 dB without it.

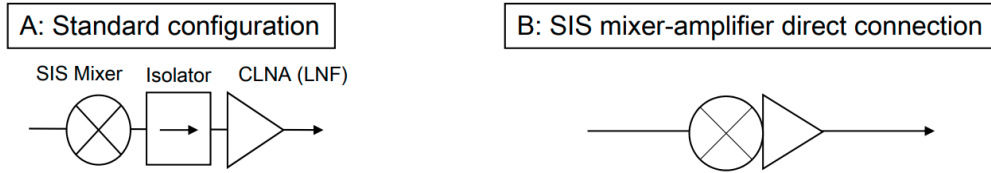


Figure 8: SIS connection with IF amplifier. A - with isolator. B - without isolator

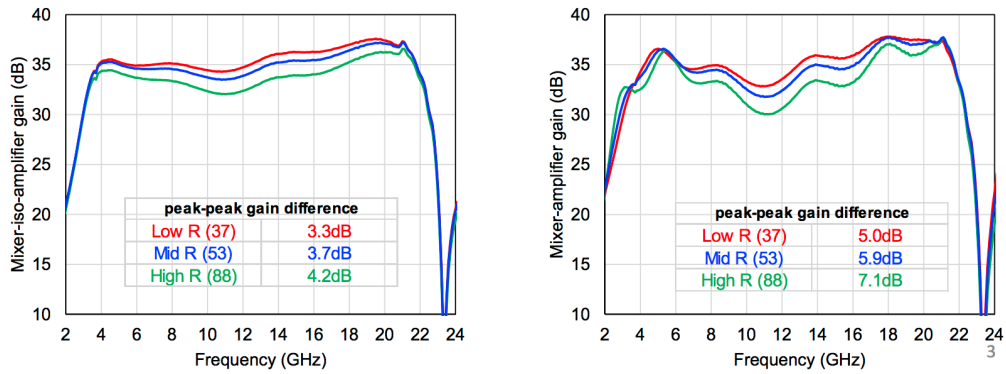


Figure 9: Preliminary simulation of the IF gain for the schemes shown on the previous figure.

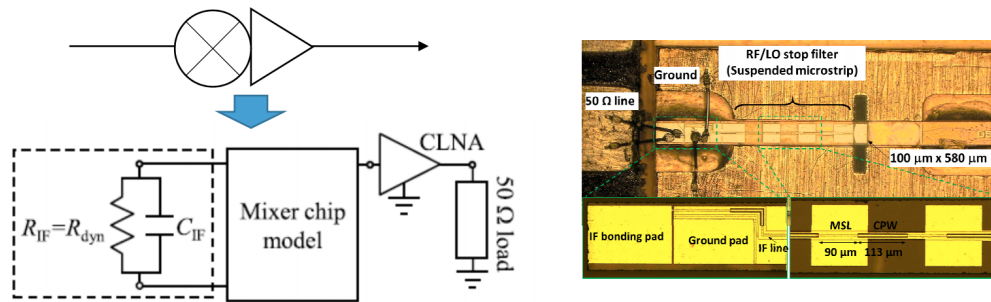


Figure 10: Mixer configuration and equivalent circuit (left side). All the circuit element (LPF, matching circuit for RF and IF) in the mixer chip are taken into account. The photograph on the right shows the mixer chip installed in the mixer block (right side).

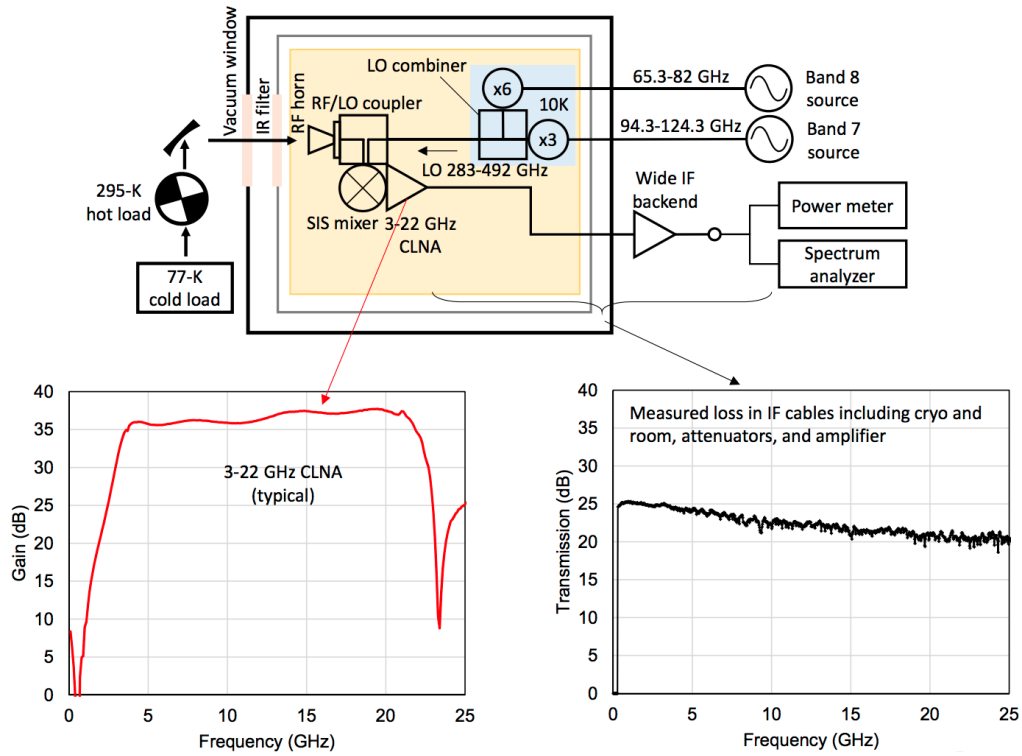


Figure 11: Measurement setup for evaluation of the 275-500 GHz DSB SIS mixer performing IF of 4-22 GHz. Plot at the bottom show performance of the cold IF amplifier and the gain of the rest of IF chain.

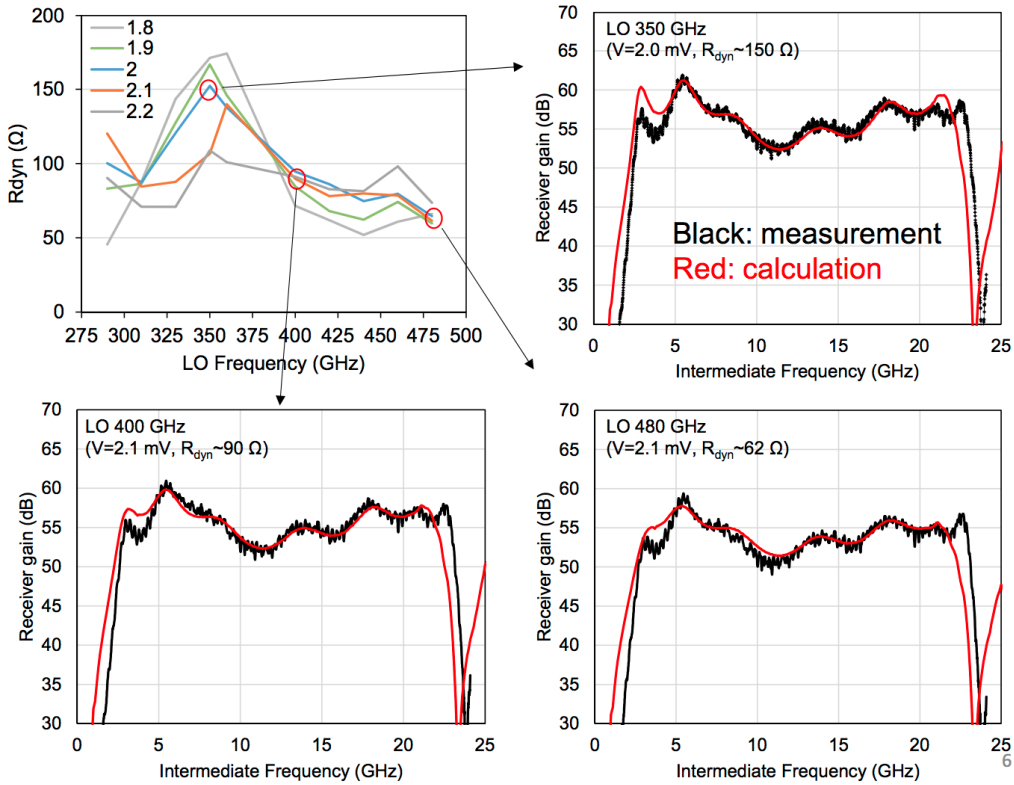


Figure 12: Comparison between measurement and calculation. The calculation includes all the loss/gain in RF/IF components.

To verify calculation, the gain has been measured using receivers shown in figure 10. Measured mixer chip used for this verification has SIS junctions with critical current density of $J_c = 30\text{kA/cm}^2$ and normal resistance of $R_n = 7.4 \Omega$ (twin junction connected in parallel). The mixer configuration and equivalent circuit used for detailed simulations are shown on the same figure on the left side. The measurements were performed using the setup shown on the scheme in figure 11. The IF spectra of the mixer gain were measured at different LO frequencies. The results for 3 LO points are shown in figure 12 (black curves) in comparison with calculations (red curves).

From figure 12 we see, that current receiver configuration (i.e. without isolator) has IF ripple up to 10 dB, making it few dB worse than prediction of detailed theoretical model. Comparing schemes with and without the isolator (see figures 8 and shown in figure 9), one can expect improvement of the measured ripples by 3dB in case a wideband isolator will be used or wideband amplifier with low S_{11} will be developed. The improvement will be feasible even based on current existing technologies with respect to the isolator and LNA. For instance, an wideband edge-mode isolator developed at Harvard-Smithsonian showed S_{11} and $S_{22} < -20$ dB, $S_{21} < -1$ dB, and $S_{12} < -10$ dB (high freq.) across the 4-20 GHz. The isolation S_{12} at high frequencies is not great but the S_{11} of the LNA is typically below -10 dB, which will not be an issue.

Talking about possibility to achieve 4dB ripple level in future, one should note that under the condition using an isolator, frequency dependence of IF output coupling in SIS mixer and gain variation of CLNA are critical. The existing wideband CLNA has very small gain ripple within the 0.5-1 dB, and 2 dB gain slope. It can be improved using an equalizer. The output reflection in SIS mixer is currently around 5-10 dB to 50 Ohm load depending on the frequency, which creates gain variation. To improve the variation, it will require for the output reflection level to be reduced. On the other hand, the calculation shown in here was done by using mixer parameters optimized for direct connection with the amplifier. Thus, by optimizing the mixer output parameter (e.g. dynamic resistance of the SIS junction, and mixer matching circuit) to 50 Ohm load or isolator input, the ripple level will be improved.

In conclusion, existing SIS receivers developed for potential ALMA upgrade of Band 7 and 8, providing extra wide IF of 4-16 GHz (or even 4-20 GHz), can have IF ripples only within 7 dB. It is still within ALMA specification, but 3 dB more than typical existing ALMA Band 8 receiver with IF 4-8 GHz. However, as mentioned above, the mixer design in this consideration is optimized for the SIS-mixer-amplifier direct connection. The ripple level for the wide IF receiver can be improved by optimizing the mixer output parameter (e.g. dynamic resistance of the SIS junction, and mixer matching circuit) to the 50 Ohm load. Thus, One can expect that after several years development the wide IF receivers will be improved and will reach also 4dB ripple level. Based on that example, the conservative prediction is saying: *due to demand of wide IF band the IF ripple for future receivers will be very similar to the one for existing receivers with IF of 4-8 GHz, unless some breakthrough technology will be developed and deployed.*

3.3.2 Image Rejection Ratio Analysis (based on 600-720 GHz 2SB receiver SEPIA660 for APEX telescope)

The image rejection ratio (IRR), which is also called a sideband rejection ratio, or even just sideband ratio, of existing ALMA receivers is normally within ALMA Specification 231 (> 10 dB for 90% of the IF range and > 7 dB over 100% of the IF range). There are known cases when some receivers were requested for waiver on IRR parameter, i.e. it was not entirely trivial to fit this specification. The IRR level of ALMA receivers is on average much better than 10 dB [4], but almost for all of them it is approaching 10 dB level at some frequencies of the RF band.

A remarkable progress in improvement of IRR of 2SB SIS mixers has been demonstrated recently by SEPIA660 receiver [5] [6]. It has been installed on APEX telescope and commissioned in 2018. It shows the IRR performance better than 15dB for more than 95% of each IF band and above 13 dB in the entire ALMA Band 9 range 600-720 GHz (see figure 13).

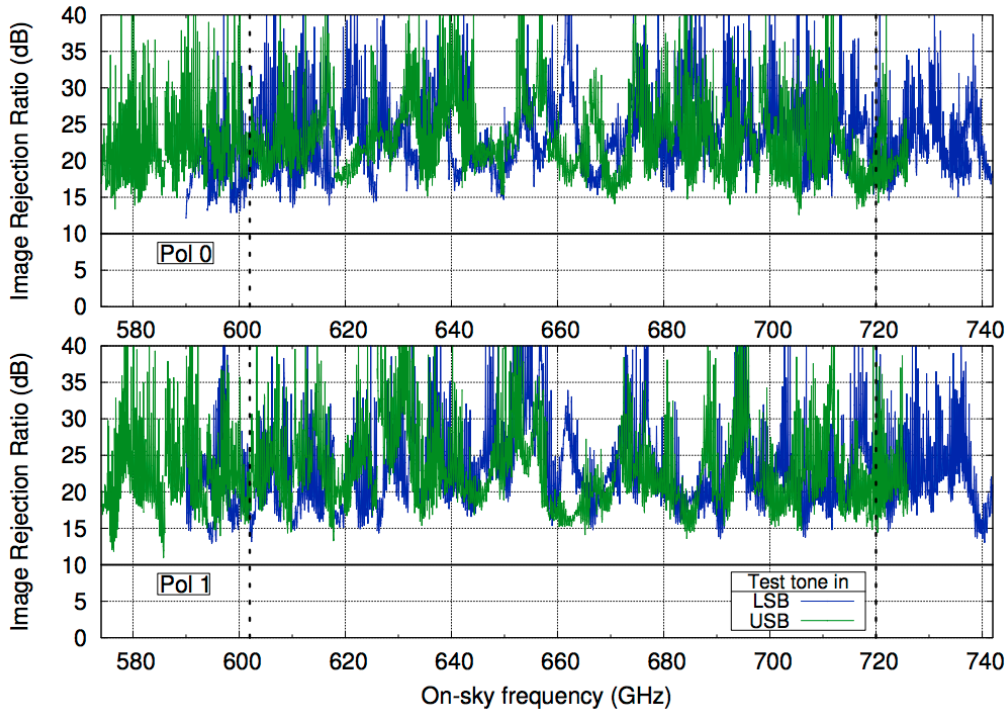


Figure 13: The image rejection ratio of SEPIA660 instrument as function of input frequency for both polarizations, and over the extended frequency band (vertical dashed lines). The horizontal axis refers to frequencies within the sideband that does not contain the test tone, i.e., the sideband used for observation. The ALMA specification is 10 dB (horizontal line)

Important to note, that the IF range is 4-12 GHz, which gives twice wider IF band than current ALMA receivers. This result was achieved due to:

- SIS mixers matching. The delivered two 2SB mixers was a result of selection out of 20 single-ended mixers, fully fitting the ALMA Band9 DSB specification. The main focus in matching was on having the same dependencies of DSB mixer gain and DSB noise temperature vs RF frequency (more details in [6]). Deviation in gain of the approved mixers, delivering top IRR performance, was not more than 1 dB. This number can be advised as a selection criteria.
- New knowledge of RF waveguide design. Focus on improvement of RF Hybrid isolation (it was reduced to level below -23 dB [6]) and additional reduction of the RF load reflections (extra losses of about 8 dB were introduced by adding a 20 mm section of the waveguide covered with Ti, details in [7]).
- State-of-the-art 4-12 GHz cryogenic IF hybrid from YEBES: improved of isolation (<25 dB), return losses (<25 dB) and balance.
- IF amplifiers with low input reflection ($S_{11} < 12$ dB).

The developers of SEPIA660 have delivered in the past ALMA Band 9 cartridges and Band 5 ones. Based on this experience, their optimistic estimation for the IRR level, which could be guaranteed for serial production of 2SB Band 9 receivers similar to SEPIA660, is as following: >15 dB for 90% of the IF range and >10 dB over 100% of the IF range, i.e. 3 to 5 dB above the existing ALMA specification for IRR for 2SB receivers. It should be noted, this will require serious effort in mixer testing and selection.

Our temporary conclusion is that the specification for ALMA on IRR could be tightened in 10 years from now by 3-5 dB, i.e. to >13-15 dB for 90% of the IF range and >10-12 dB over 100% of the IF range, presuming that: 1) instrumentation groups will learn from each other tips on improvement of IRR of 2SB SIS mixers; 2) current state-of-the-art technology for cryogenic amplifiers, IF hybrids and SIS mixers for 4-12 GHz IF will be extended to 4-16 GHz IF or further;

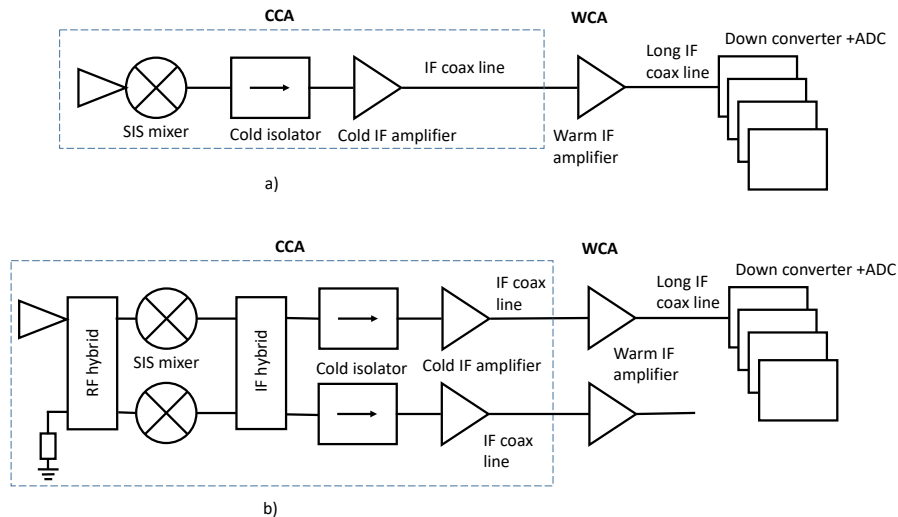


Figure 14: ALMA front end receiver signal flow diagram for ALMA band 9, 10 DSB receivers, a) and for ALMA bands 3, 4, 5, 7, 8 2SB receivers, b). Only one polarization channel is shown

3) amount of resources (cost, time, expertise) available for new cartridges will not be less than in the past, because serial production of cartridges with such a quality will require additional effort in SIS mixers selection and special attention to quality of all components.

3.3.3 IF pass band ripple analysis

Digital front end implementation will allow for substantial increased of processed RF/IF bandwidth. In order to support such a bandwidth, current ALMA front end cartridges should be upgraded. This necessary modification will make an opportunity to replace critical analogue components of ALMA system by modern better quality elements. We consider components such as wide band SIS mixers, cryogenic IF amplifier, IF hybrid, IF isolator. Most important improvement that we can analyze here is system band pass ripple budget. As discussed in section 4.1.1 an instantaneous dynamic range of 5.6 ENOBs is required while 4 ENOBs is required for correlator, the rest of 1.2 ENOBs (6.12 dB) can be used to accommodate change of IF power within pass band. With current ALMA analogue pass band ripple requirements of 12 dB several digitization options lack the required dynamic range.

3.3.3.1 Ripple analysis

First let us consider pass band ripple. ALMA front end consists of several components interconnected with a 50 Ohm IF lines. Typical signal chain configurations for ALMA mixers are shown in figure 14,15. ALMA front end receiver consists of a cold cartridge assembly (CCA), warm cartridge assembly (WCA) and IF switch/down converter/ digitizer modules. The CCA have a certain physical size with SIS mixer located on top of it which dictates the length of coaxial cables between SIS and cold amplifiers as well as between cold amplifier and WCA warm IF amplifier. Very long coaxial line is used between WCA and IF switch/down converter. We have three typical signal configurations:

- a DSB configuration as shown in figure 14 a),
- a 2SB configuration as shown in figure 14 b),
- a 2SB configuration with integrated SIS mixer and IF amplifiers as used for ALMA band 6 presented in figure 15 a),
- an RF preamplified 2SB configuration with down converter in WCA at room temperature that will be used for ALMA band 2 shown in figure 15 b)

ALMA band 1 is using classical single side band configuration where the band is determined by RF filter. Its scheme is similar to one presented in figure 15 b), where a DSB IF down converter

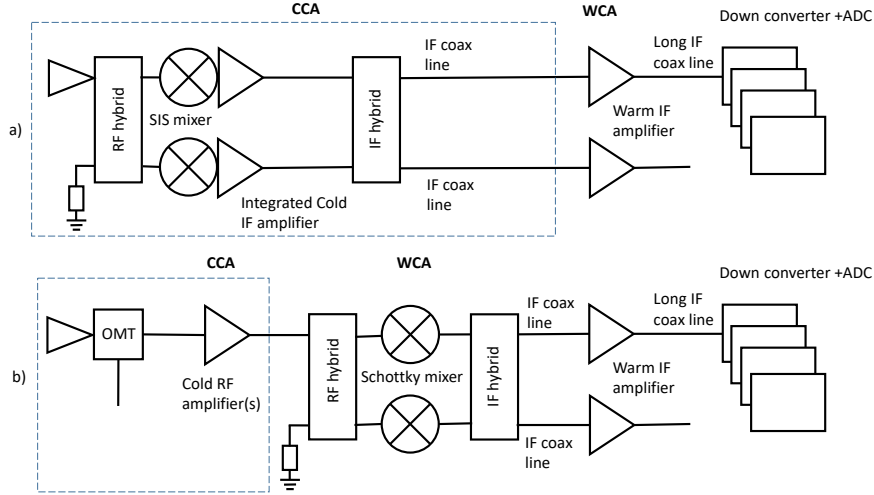


Figure 15: ALMA front end receiver signal flow diagram for ALMA band 6 2SB receivers with integrated SIS mixer/IF amplifiers, a) and signal flow diagram for for ALMA band 2, b) Only one polarization channel is shown.

is used to instead of 2SB. Typical front end signal chain contains 6 IF components connected with each other with cables of various lengths. All of these components are not ideal and has an input and output reflection and its own intrinsic pass band ripple. While intrinsic pass band ripple of each component can be minimized during its design phase, input and output mismatch is a system issue which we characterize here. The pass band ripple R_{BP} as ratio of maximum to minimum transmission from component 1 to component 2 through a 50 Ohm coaxial line is related to output return loss $|S_{22}|$ of component 1 and input return loss $|S_{11}|$ of component 2 by the following expression:

$$R_{BP} = \frac{(\sqrt{|S_{11}|}\sqrt{|S_{22}|} - 1)^2}{(\sqrt{|S_{11}|}\sqrt{|S_{22}|} + 1)^2} \quad (10)$$

The ripple given in eq. (10) and calculated for different values of $|S_{11}|$, $|S_{22}|$ is shown in Figure 16 which demonstrates demonstrates that in order to achieve a low ripple over transmission line a relatively low return loss is required. A poor match on one side of the transmission line can be compensated by better match, i.e. lower $|S_{11}|$ on the other side of the connection. This is especially visible if we express the required $|S_{22}|$ as a function of $|S_{11}|$ for given required ripple as

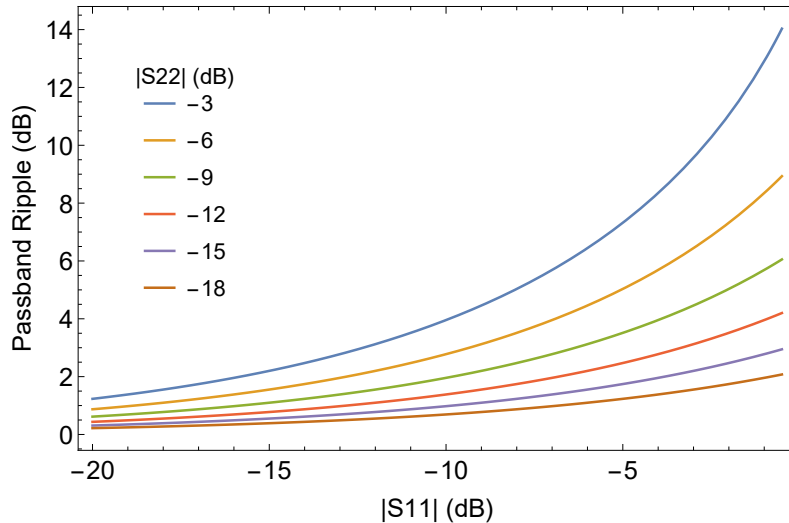


Figure 16: The ripple given in eq. (10) and calculated for different values of $|S_{11}|$, $|S_{22}|$

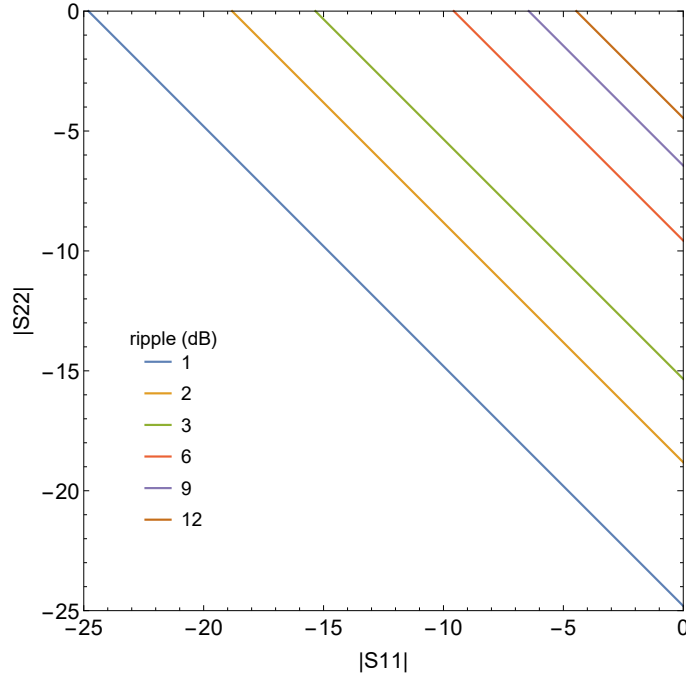


Figure 17: pass band ripple $|S_{22}|$ as function of $|S_{11}|$ for different ripple R_{BP} values as calculated from inverting equation (10)

shown in figure 17.

In order to create a ripple budget we need to assume a S_{11} , S_{22} values for different components in the signal chain as shown in the following table 12. We assume that ripple pattern in each cable is not related between components and we calculate resulting ripple by adding squares cable and components ripples in square. Total maximum ripple is calculated by adding the individual ripple values. The cable ripple between components has been calculated using (10). For this version of table a theoretically achievable values for wide band components have been used. For these values total average ripple can be as low as 1.81 dB which is a much better value in comparison with ripple specifications of 12 dB achieved by current ALMA. Components with such characteristics are not available in the market at this moment but can be developed over course of time. This development and possible tighter manufacturing tolerances and additional testing and lower yield will result in much higher price per components.

3.3.3.2 SIS mixer output match estimates

We consider the IF ranges of 4-20 GHz here. The main uncertainty parameter in table 12 is SIS junction output $|S_{22}|$. This parameter can be estimated by noting that SIS mixer output impedance can be modeled by parallel connection of SIS junction geometric capacitance C_{SIS} ,

Table 12: System components achievable ripple budget

Component	S_{11} (dB)	S_{22} (dB)	comp. ripple	cable ripple
SIS mixer	-	-10	-	0.7
IF hybrid	-18	-18	0.2	0.27
Isolator	-18	-18	0.2	0.7
Cold IF Amplifier	-10	-18	1	0.27
Warm IF Amplifier	-18	-18	1	0.27
IF switch	-18	-	-	
Total				1.81
Total max				4.6

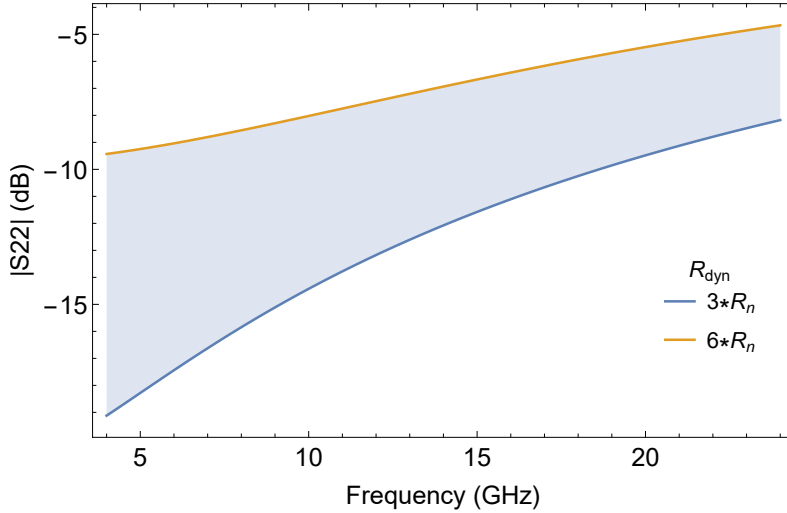


Figure 18: Output receiver S_{22} in case of ALMA band 9 DSB mixer. Used parameters, $R_n A = 7 \text{ Ohm } \mu\text{m}^2$, $C_{sp} = 80 \text{ fF}/\mu\text{m}^2$, $C_{par} = 80 \text{ fF}/\mu\text{m}^2$, $A = 1 \mu\text{m}^2$. See text for model and explanations.

parasitic capacitance of layout C_{par} and SIS junction output resistance R_{dyn} . C_{SIS} depends on product SIS junction specific capacitance C_{sp} and junction area A : $C_{SIS} = A * C_{sp}$. SIS junction output resistance R_{dyn} depends on LO frequency and operating point of SIS mixer. Typically it ranges within $R_{dyn}=3..6 \cdot R_n$ for ALMA band 9 mixer, where R_n is normal resistance of SIS junction. For SIS junction of a given area R_n is given by $R_n = R_n A * A$, where $R_n A$ is junctions $R_n A$ product, which is a characteristics of SIS junction barrier and depends on type of the tunnel barrier used. For high current density AlN barrier SIS junction $R_n A$ ranges from 1 to 20 $\text{Ohm} * \mu\text{m}^2$ and for AlO_x tunnel barrier $R_n A$ is within 20..60 $\text{Ohm} * \mu\text{m}^2$. For a wide RF bandwidth SIS mixers $R_n A$ values are typically chosen in the lower available range because inherent RF bandwidth depends on the product of $R_n * C_{SIS} = R_n A * C_{sp}$ which is independent on junction area.

The SIS junction output match $|S_{22}|$ for ALMA a typical band 9 DSB mixers with AlN tunnel barrier technology is presented in figure 18. In this case, SIS junction is directly connected to a 50 Ohm transmission line, avoiding any impedance transformation. This allows to use longer transmission lines to connect to other components. The range, presented in the figure 18 corresponds to a -5..-10 dB S_{22} in the worst case and -15..-10 dB as typical values, see figure caption for parameters used in the calculation. The mixer's S_{22} depends critically on junction's area and $R_n A$ product. These parameters do vary from junction to junction for A and from batch to batch in case of $R_n A$ product, which can easily produce a spread of $\pm 5\text{dB}$ in S_{22} both in upper and lower. The parasitic capacitance value depends on particular design and in practice can not be made sufficiently smaller, especially for lower frequency bands.

In conclusion the SIS $|S_{22}|$ can not be made much smaller than -8 dB for higher end of considered IF band of 4-20 GHz which will always limit the ripple budget for the 50 Ω system. These values are also confirmed for a wide band mixer for ALMA band 8 presented in section 3.3.1. specifications of other components in signal chain must be tightened to improve the current ALMA ripple specifications. The SIS $|S_{22}|$ for lower ohmic system can still be better for the same SIS junction area and specific capacitance. This lower impedance will need to be transformed over very large fractional bandwidth to a standard 50 Ω impedance to be able to carry over large distance using cables. This impedance transformation itself brings limitations in system ripple. The benefits of such approach for improving system ripple needs to be carefully analyzed.

3.3.3.3 System ripple mitigation

While system ripple budget critically depends on input/output match of components, there is another parameter which is of importance: distance between components. If mechanical/electrical layout allows, distance between components can be reduced below $\lambda/4$ in the connecting transmission for the highest design frequency. This will result in converting the ripple, i.e. variations of

signal transfer with several minima and maxima within IF bandwidth into a slope, i.e. monotonic linear variation across the band. The system slope of different components add up or subtract but remain a linear slope. This slope is typically constant for a given ALMA front end cartridge signal chain with only small variations due to different R_{dyn} for a different LO frequencies in SIS mixer. Long cable losses are also contributing to the system slope. System slope is not varying to large extend from one unit to another with the same design, thus it can be reduced with a coaxial slope corrector. These small size coaxial components are commercially available for slopes values and can be used in ALMA system so far it is fixed. Furthermore, each cartridge system of the same can be easily fitted with an individual slope corrector with fitted value at warm amplifier output level after standard cartridge band-pass response measurement.

As removing system slope is relatively straight forward in component integration with each other, this can be considered as a good way to improve the system ripple. The typical $\lambda/4$ value is 2.7 mm for 20 GHz in a mostly widely used coaxial cable. This distance does still allow to use discrete SIS mixer and discrete IF amplifier located in the same mixer block, but this practically excludes interfacing them through commercially available 50 Ohm coaxial connectors. One should also note that for integration, distance between reflection defining elements, SIS mixer and the input transformation stage of an IF amplifier should be kept shorter than 2.7 mm, which is practically impossible for any discrete components based cold IF amplifier and can be confirmed by analyzing ripple performance of current ALMA band 6 system which uses direct integration of SIS mixer and IF amplifier at 2 times lower IF frequency than one which is considered here.

One practical direction for integrating components is MMIC design, i.e. combining several components on one chip and, in case of SIS mixer/amplifier, integrating an MMIC amplifier chip into mixer block. Then the transmission line between a SIS mixer and an amplifier transistor stage can be kept small enough. MMIC's also allow to use many more of much smaller components to provide for flattening the pass band of the system. The same MMIC solution can also be considered in any part the system because MMIC's can include a lot of functionality on one chip resulting in the reduced component count. Another advantage of this solution is that the ripple/slope performance of an MMIC is typically more stable chip to chip and can be mitigated by a fixed microwave circuit. For disadvantages, one can list challenging thermal design in case of integration with SIS junction at 4K level due to several orders of the magnitude difference of the device dissipation levels in a HEMT technology v.s. a SIS junction. Another disadvantage is the relatively high NRE cost for an MMIC design and development due to high cost of technological tape-outs. However, if the NRE cost are done by industry, MMIC components are usually significantly cheaper than discrete integrated parts due to a much lower manpower effort needed to produce the final component. While for typical numbers ($70 \times 4 \approx 300$ in case of the low noise and the first warm amplifier units) in ALMA the NRE for custom MMIC design are about cost neutral, off the shelves MMIC components must be always considered. *It must be noted, that for the extremely large relative IF bandwidth considered here, the MMICs can be the only practical solution and is hard to avoid. It can be illustrated by the fact that the best low noise amplifiers, for instance from Low Noise Factory (LNF) are MMIC based.*

A classical way of reducing system ripple is by using fixed attenuators in between reflecting components. These can be relatively inexpensive and an attenuator lowers $|S_{11}|$ at the component level by twice their attenuation value in dB, providing the resulting $|S_{11}|$ is not lower than the reflection coefficient of the attenuator itself. It is important to notice that many required $|S_{11}|, |S_{12}|$ are below -18 dB and a high quality grade attenuators are required those are more expensive. Another disadvantage of this method, which is similar to the use of slope correctors, that both require an additional amplification, which also comes at the additional cost. Attenuators can not be used between SIS mixer and IF amplifier because both components define the noise temperature of the system. It can be easily demonstrated that system performance in terms of overall system sensitivity depends much stronger on mixer noise temperature than on system digitizer dynamic range.

Additionally, reducing the component count is also a good measure to reduce system ripple/slope. A typical example of such an approach has been discussed in digital channel switching using optical fibers, see figure 27 in section 4.3. Another example which is discussed in the same section is using an individual digitizer module per each analogue channel of the ALMA cartridge which allows to shorten IF cables and also will allow to improve the stability of the system.

Finally, another good way to reduce component count is to reduce number of coaxial interfaces in the system. This can be achieved by integrating components on one printed circuit board, using

lumped elements or microstrip or CPW lines as transmission line alternatives.

Many of the above mentioned measures has been already adopted in the ALMA signal chain design and for the component selection. The main reason to revisit this question is due to the tightening ripple/slope specification which is needed for the full band digitization at once with its relatively limited dynamic range.

4 Digital Front-End Architecture

In general, there is a trade off between processing power in the antenna and the bandwidth required between the antennas and the correlator. For example: performing digital sideband rejection and bandpass ripple equalization on 8 bits (6.5 ENOBs) samples on antenna, allows requantization to 4 bits before transmitting the data over the fiber, while keeping a very high (98%) of quantization efficiency. If there is no processing power in the antenna this would require significantly more bits to be transmitted to the correlator in order to reach the desired overall quantization efficiency in spite of the passband level variation. Since most of the pre-processing, filtering and calibration techniques are more naturally implemented in the frequency domain, we here advocate for having at least a coarse channelizer at the antenna. This FFX architecture is one of the options discussed. There is still an open debate about the trade-offs of having the entire F engine in antenna, i.e. implementing an FX correlator. This architecture, plus the use of IP addressing (GBE switches), would allow a natural implementation of multiple, independent X engines, on-demand sub-array configurations, GPU-based software correlators, and high resolution time domain machines.

4.1 Quantization efficiency and Impact of gain variations within the pass band

4.1.1 Quantization efficiency and digitizer response versus threshold spacing

Before embarking on a discussion of quantization efficiency, it is worth emphasizing that the quantization resolution requirement #521 is critical to the overall effectiveness of ALMA and the exact value of this requirement should be decided on the basis of a cost-benefit analysis: **for example, comparison with the approximate known cost of a fully equipped antenna leads to the benchmark that a 1% improvement in sensitivity is "worth" 8 MUSD.**

The main goal of this section is to define in general terms the quantization efficiency of an analog-to-digital converter (ADC) to show how it varies with the number of bits and the quantization threshold. This is independent of any selected ADC architecture or technology and essential to estimate the headroom above the noise level (Table 13) and the ADC dynamic range (Table 14). The main characteristics of the fastest commercial ADCs of interest to this study are discussed in section 5.3.

Assuming equal quantization threshold (or level spacing), s , in units of σ the *r.m.s.* noise prior to signal quantization, then, the maximum voltage range at the sampler input is $\pm m.s$ for an n -bit sampler providing $2m = 2^n$ levels. Quantization adds noise prior to signal processing and one defines the quantization efficiency, η , as the ratio of the signal-to-noise ratio with and without quantization. In general, one adjusts the threshold spacing so that the quantization efficiency is maximum, i.e. $\eta = \eta_{max}(s_0)$ for $s = s_0$. However, selecting a value of s larger than s_0 may result, for a given number of bits, in a broader voltage range accepted by the sampler quantizer while the efficiency is little degraded.

We have used the formula from Thompson et al. (2007) [8] to derive (Fortran programming) and plot the quantization efficiency versus the parameter s . Up to 1000 individual values of s have been used to generate the efficiency output files; ‘oversampling’ of the parameter s is necessary to precisely identify the maximum efficiency. Figures 19 and 20 show the efficiency for 2- to 7-bit and 2- to 12-bit digitization in the range $s = 10^{-2}$ to 2 and 10^{-4} to 2, respectively. When s tends to zero the efficiency tends to the limit $2/\pi$. It is clear from these plots that above 5 bits, adjusting the threshold spacing is not critical to achieve a high efficiency.

We derive here: a) the maximum voltage range accepted by an n -bit sampler for different threshold spacings and b) the n -bit sampler dynamic range for a minimum value of the quantization efficiency using our efficiency output files.

a) In Table 13 we give examples of the maximum voltage range $\pm m.s.\sigma$ for a total of $\pm m$ levels ($2m = 2^n$) above the *r.m.s.* noise at the digitizer input. This is derived in dB for $n = 3$ to 12 bits from the difference $\pm(20\log(m.s.\sigma) - 20\log(\sigma)) = \pm 20\log(m.s)$. Table 13 thus indicates for different values of the threshold spacing if signal peaks well above σ or if interfering signals could be ‘detected’ by the quantizer of an n -bit sampler. We also give in Table 13, using our efficiency output files, the shift from the maximum efficiency resulting from s being different from s_0 . This is derived from $\Delta\eta = (\eta_{max}(s_0, n\text{-bit}) - \eta(s, n\text{-bit}))$.

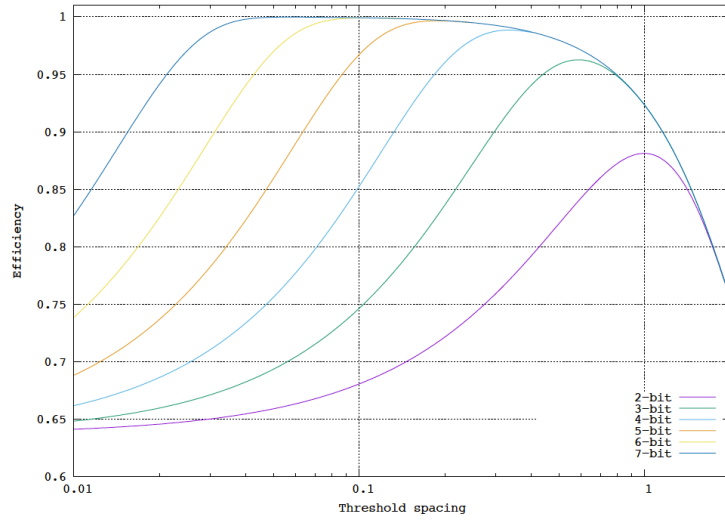


Figure 19: Quantization efficiency versus the threshold spacing (in units of the r.m.s. noise prior to quantization) in the range 0.01 to 2 for $n = 2, 3, 4, 5, 6$ and 7 bits.

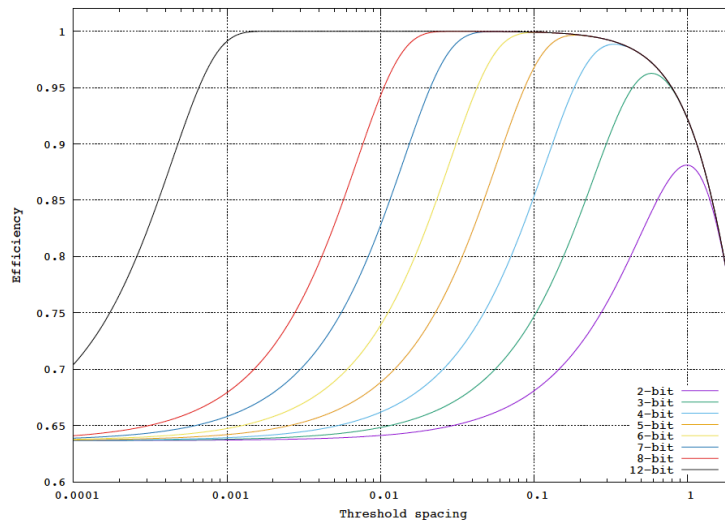


Figure 20: Quantization efficiency versus the threshold spacing (in units of the r.m.s. noise prior to quantization) in the range 0.0001 to 2 for $n = 2, 3, 4, 5, 6, 7, 8$ and 12 bits.

Table 13: Maximum voltage range above noise level (in dB) for different n -bit digitizers and threshold spacings (the spacing parameter, s , is in units of the r.m.s. noise prior to quantization). The shift from the maximum efficiency, $\Delta\eta$, for a given value of the threshold and for different bits is also estimated (in %).

Max. voltage range above input noise $\Delta\eta$ Spacing parameter	3-bit $\eta_{max} = 96.3\%$	4-bit $\eta_{max} = 98.8\%$	5-bit $\eta_{max} = 99.7\%$	6-bit $\eta_{max} = 99.9\%$	12-bit $\eta_{max} = 100\%$
1.0	± 12.0 dB ~ 4 %	± 18.1 dB ~ 6.5 %	± 24.1 dB ~ 7 %	± 30.1 dB ~ 8 %	± 66.2 dB ~ 8 %
0.6	± 7.6 dB ~ 0 %	± 13.6 dB ~ 2 %	± 19.6 dB ~ 2.5 %	± 25.7 dB ~ 3 %	± 61.8 dB ~ 3 %
0.3	± 1.6 dB ~ 6 %	± 7.6 dB ~ 0 %	± 13.6 dB ~ 0.4 %	± 19.6 dB ~ 0.6 %	± 55.8 dB ~ 1 %
0.2	± 1.9 dB ~ 13 %	± 4.1 dB ~ 3 %	± 10.1 dB ~ 0 %	± 16.1 dB ~ 0.2 %	± 52.2 dB ~ 0.3 %
0.1	± 8.0 dB ~ 22 %	± 1.9 dB ~ 13.5 %	± 4.1 dB ~ 3 %	± 10.1 dB ~ 0 %	± 46.2 dB ~ 0.1 %

b) In Table 14 we give the input voltage variation (in dB) above a fixed value of the efficiency from the range of threshold spacings compliant with the minimum efficiency for different values of n . Table 14 thus gives the maximum dynamic range for a minimum value of the efficiency.

Table 14: Sampler dynamic range for a minimum quantization efficiency.

n-bit	2-bit	3-bit	4-bit	5-bit	6-bit	7-bit	8-bit	12-bit
99%	-	-	-	8.4 dB	14.7 dB	20.9 dB	26.8 dB	51.0 dB
96%	-	2.2 dB	11.0 dB	17.5 dB	23.7 dB	29.8 dB	35.9 dB	60.0 dB
92%	-	9.5 dB	16.7 dB	23.1 dB	29.3 dB	35.4 dB	41.4 dB	65.6 dB
85%	6.9 dB	16.5 dB	23.4 dB	29.8 dB	35.9 dB	42.0 dB	48.0 dB	72.2 dB

The results in Table 14 are shown in Figure 21 . For a given number of bits, there is a monotonic decrease of the maximum input voltage range versus the minimum efficiency until this range reaches zero when the efficiency reaches its maximum value (this is nearly 0.96 and 0.99 for the 3- and 4-b cases, respectively, and nearly 1 for 5 bits and beyond). Using Fig. 3 one immediately sees for example that if a minimum efficiency of 0.97 is required first, the 3-b case is not compliant and second, one can reach a dynamic range of 9, 15 and 21 dB with 4, 5 and 6 bits, respectively.

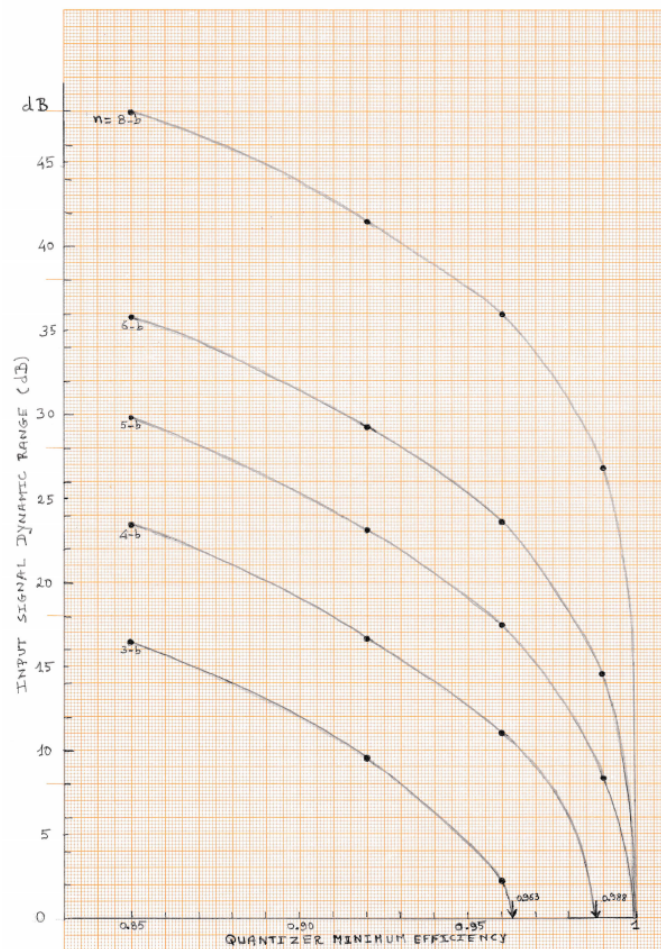


Figure 21: Input signal dynamic range (in dB) compliant with a minimum quantization efficiency for $n = 3, 4, 5, 6, 7$ and 8 bits. For a given number of bits and along a same curve the voltage range goes down to zero when the efficiency reaches its maximum. The maximum efficiency for 3 and 4 bits is shown with an arrow on the x-axis at 0.963 and 0.988 , respectively. The dots along each plot correspond to the values given in Table 14. The analog input passband is supposed to be flat.

4.1.2 Impact of gain variations throughout the signal passband

The results shown in Table 14 and in Figs. 19,20 and 21 assume that the quantization process is made for an ideal flat passband (and for equal quantization steps). In practice, there might be a slope and ripple across the passband which may decrease the efficiency and thus impact the signal-to-noise-ratio (SNR) across the passband.

The effect of quantization in digital correlators has been presented in different works. Numerical simulations were performed for three levels by Lamb in 2002 [9] and, for the full 3-b, 8-level case, by Carlson and Perley in 2004 [10] assuming that the quantization noise is spread throughout the passband. These works show that the frequency dependence of the input power impacts the SNR of the correlation coefficient and that the efficiency decreases when the gain slope is lower. For broad-band signals these studies help in deciding when gain equalization is desirable. The nature of the quantization noise has further been studied by Thompson and Emerson in 2005 [11]; numerical experiments showed that the power spectrum of the quantization noise is nearly flat across the receiver passband even though the input power spectrum may vary significantly. This is especially important for line observations made with a broad-band system since if the SNR does not remain uniform across the passband the interferometer maps may not have comparable dynamic range. (We also note that Thompson [12] has estimated the sensitivity degradation of an interferometer resulting from a bandpass slope in the simple case where there is no digitization and for a single channel. The loss is similar to that of a single dish with a non-flat input passband which may

decrease the 'effective bandwidth' - see chapter on radio receivers in [13] - and, hence, decrease the SNR.)

Because the ratio of the variance of the unquantized signal at one input of the correlator to the variance of the same signal after quantization directly gives the efficiency as defined at the beginning of this memo, there is a simple relationship between the power spectral density at two different points in the passband, the ratio of the signal-to-noise R_{SNR} at these two points and digitization efficiency. (It is further assumed that the quantization noise and the signal noise can be added as two Gaussian signals.) One can estimate:

1. the SNR loss, for a given efficiency, resulting from a passband slope between two power spectral points;
2. the acceptable variations in the passband at the input of the quantizer assuming that the value of R_{SNR} does not exceed an adopted value.

Case(1): P_1 and P_2 being the signal power spectral densities at two different frequencies in the passband and writing $P_2 = rP_1$ with, for example, $r < 1$ (i.e. there is a decreasing slope from P_1 to P_2), then, using the signal and noise variances to define the efficiency, we derive

$$R_{SNR} = SNR(P_1)/SNR(P_2) = [1 + 0.5(1 + 1/r)(1/\eta - 1)]/[1 + 0.5(1 + r)(1/\eta - 1)]$$

In Fig. 22 we plot R_{SNR} for different quantization schemes (corresponding to different values of η) and for different bandpass slopes (given in dB by $10 \log r$). Fig. 22 also gives the SNR loss in % at the lower end of the power spectral density (i.e. the loss at P_2 which is simply the complement to $1/R_{SNR}$ to reach 100%). Passband slopes from -0.5 to -6 dB have been considered here. For a fixed value of the quantization efficiency, R_{SNR} increases above 1 with increasing values of the passband slope. Consider, for example, two slopes of -6 and -0.5 dB (i.e. $r = 0.25$ and 0.89), we obtain a SNR loss of -7.1% and -0.5% assuming $\eta = 0.96$ (ideal 3-b quantization). For η around 0.99 and for the same slopes the SNR losses would be -1.9% and -0.12%, respectively. Fig. 22 can also be used to estimate the efficiency required to accept a maximum SNR loss for a given passband slope. Assuming we wish to achieve an SNR loss better than 2% then, if the slope is corrected to within 3 dB, the efficiency must be better than 0.97. If the slope is corrected to within 1 dB the efficiency is relaxed to 0.91.

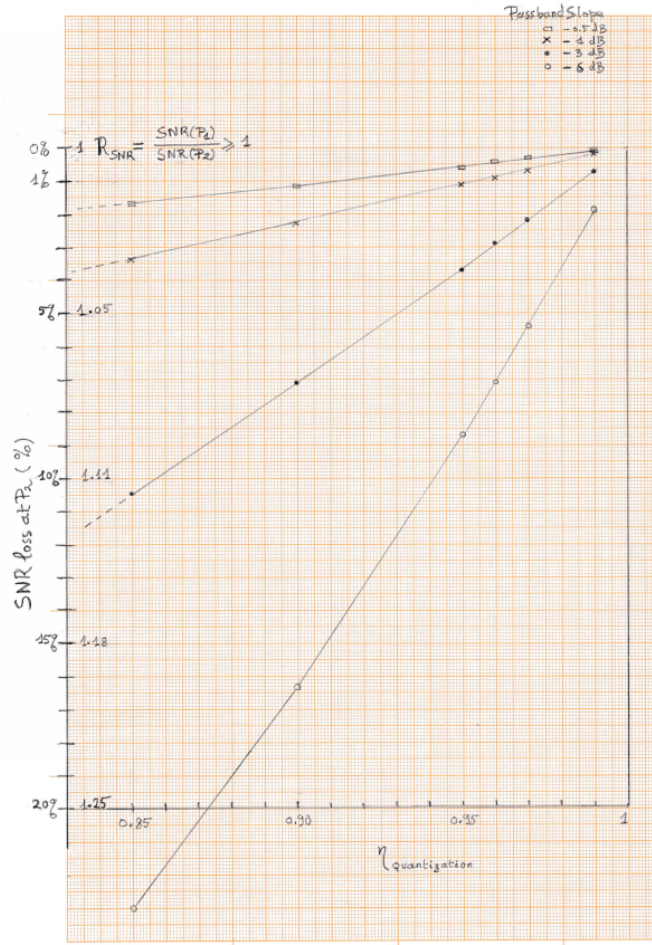


Figure 22: SNR loss for different quantizers and different monotonical slopes throughout the input power passband. -0.5, -1, -3 and -6 dB slopes have been considered.

Case (2): Assuming there is a trough in the power spectral density, P , with respect to the average power density, P_{av} , one can plot the ratio P/P_{av} for different values of h and for a ratio $R_{SNR} = SNR(P)/SNR(P_{av})$ not exceeding a reasonable fixed value. This is described by the equation

$$P/P_{av} = (1 - \eta)/(1/R_{SNR} - \eta)$$

and plotted in Fig. 23 for two moderate SNR losses corresponding to $R_{SNR} = -0.5$ and -1 dB (or 0.89 and 0.794).

Fig.23 can be read in different ways. For a given quantization scheme (or a fixed value of the efficiency) the power variation acceptable at the correlator input is larger if one accepts a larger degradation in R_{SNR} . Considering for example an efficiency around 0.96 the power variation which can be tolerated with respect to the nearby average goes from -6 to nearly -9 dB if one accepts to relax the value of the R_{SNR} from -0.5 to -1 dB. Fig.23 also shows that for a constant value of R_{SNR} a higher efficiency allows to accommodate a larger power variation with respect to the nearby mean level. Assuming $R_{SNR} = -0.5$ dB a 0.99 efficiency allows a variation around -11.5 dB while it is only -6 dB at 0.96 efficiency. This clearly shows that a higher efficiency tolerates larger power variations in the input signal passband.

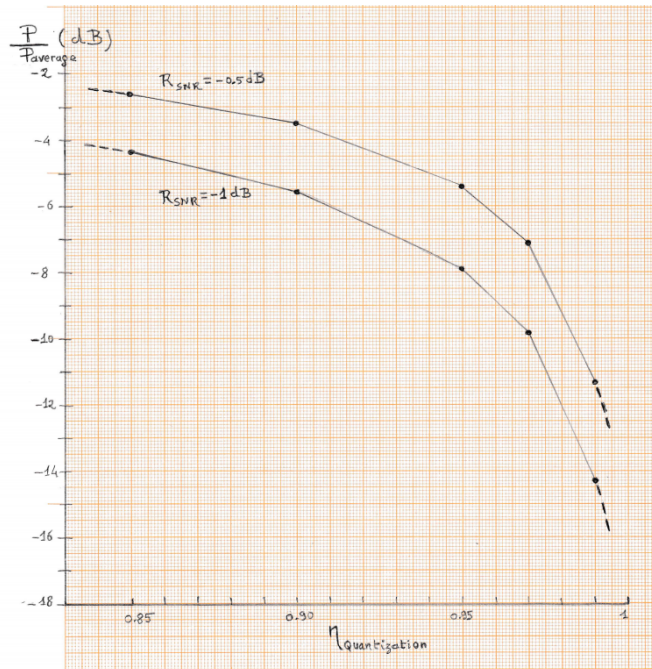


Figure 23: Power variation with respect to the mean level for different quantization schemes and for two fixed values of the SNR ratio, -0.5 and -1 dB.

4.2 Overall concept

A diagram on Figure 24 shows in simplified way the current ALMA signal processing scheme. It is followed by a block diagram of Digital Front-End concept shown in Figure 25

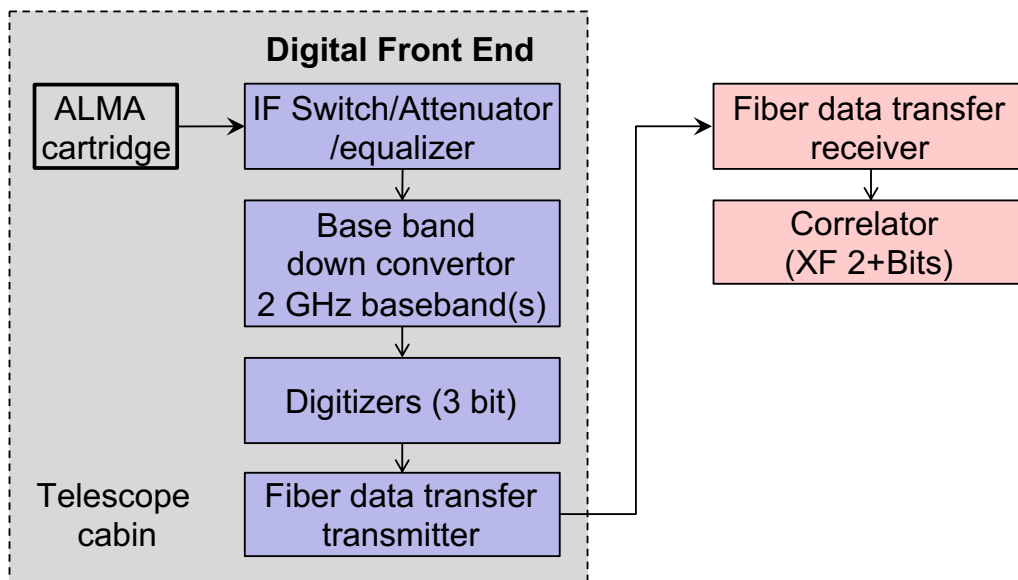


Figure 24: Current ALMA configuration.

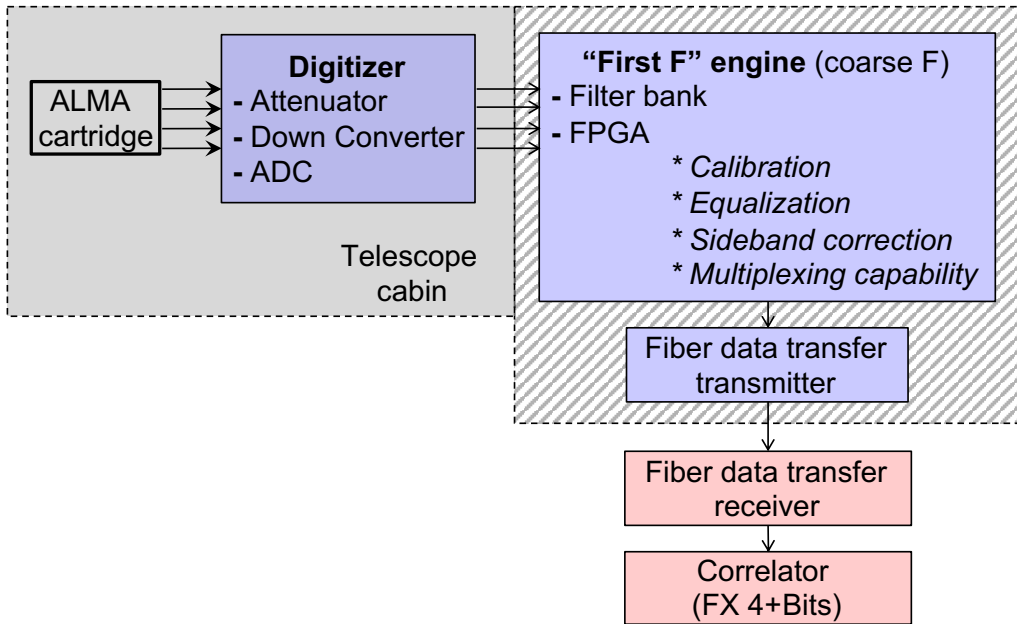


Figure 25: Digital Front-End concept. The hatched area marks the parts, which are supposed to be placed in a telescope cabin, but the option to locate them next to correlator is also under consideration.

A possible configuration for the ALMA DFE is the one suggested in the diagram below.

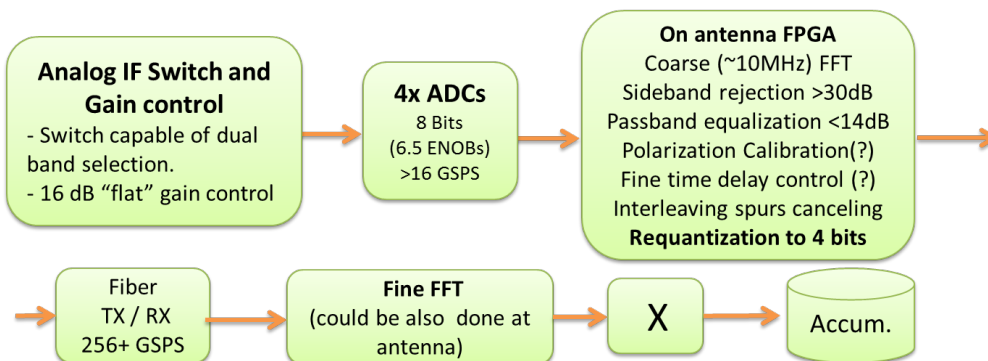


Figure 26: An example of a possible architecture.

16 dB of ‘flat’ gain control on each channel is necessary to compensate for band-to-band, cartridge-to-cartridge and RF-to-RF signal level differences. Then, 4x 25GSPS 8 Bits (6.5 ENOBs) ADCs digitize up to four 4-12 GHz IFs. An on-antenna FPGA performs a coarse (10 MHz resolution) channelization to then apply correction coefficients allowing digital sideband rejection and gain ripple (up to 14dB peak to peak) equalization. This dramatically improves sideband rejection and quantization efficiency and considerably reduces the required analog specification for sideband rejection and gain ripple/slope for new cartridges. This configuration also allows digital polarization calibration and part of digital delay tracking on antenna.

In the same FPGA the data is re-quantized to 4 bits before transmission, so that only 256 Gbps is required to transfer the payload (total data link bandwidth depends on protocol). The above configuration is able to provide 98% of quantization efficiency and 30dB of sideband rejection for any receiver. It can calibrate up 14dB of IF gain ripple within the 4-12 (4-8) GHz IF bandwidth. Possibly, a full resolution FFT could be implemented at the antenna so that only the X machine is implemented at the AOS technical building. The Ethernet switches can implement the cross connections for a number of specific-purpose correlators. In this way subarrays or specific machines (pulsar, etc) could be added by just plugging additional computing resources to the Ethernet in-

frastructure.

In general the following pros and cons can be identified for the above configuration:

Pros:

1. Minimum ADC count (1 per IF channel)
2. Minimum data rate over the fiber (256 Gbps + protocol overhead)
3. Very high (98%) quantization efficiency (>10% more than current configuration!)
4. Very high sideband rejection (for astronomical and atmospheric sources)
5. Works with existing and future receivers
6. Can be made backward compatible with existing correlator and DTS hardware

Cons:

1. Requires a high-speed ADC with >6 ENOBs which is currently not commercially available
2. Requires a calibration source for determining coefficients needed for digital sideband rejection

4.3 Modularity

Downstream of the FE cartridges, it is desirable to have a modular system that will allow the system to be easily upgraded in terms of bandwidth, processing power and number of FE cartridges.

For bandwidth, an ADC board that has a through port, a complex downconverter, two ADCs for quadrature sampling, and an digital optical transmitter will maximize modularity, see an example in figure 43. The through port allows an increase in bandwidth by adding another ADC board to the system, the downconverter will allow each ADC board to sample a different band, and the optical transmitter will enable data transmission to a processor board. Only the ADC on the cartridge in use will be transmitting data to the optical combiners, the remaining ADCs will turn off their fiber transmitters.

For processing, the optical signals from an ADC will be transmitted to a processor board that will have an optical receiver, an FPGA and an optical Ethernet transceiver (see figure 27). Each processor can be connected to one ADC board per receiver through an optical combiner, turning on the optical transmitter of the ADCs of the enable FE cartridge, and the optical transmitters of the remaining ADCs turned off. Changing the desired processing of the signal can be done by reprogramming the FPGA.

In current ALMA downconverter/digitizing implementation hardly any digital signal processing other than formatting takes place. Digitizer and formatter are on the same board and in the same rack with downconverters.

Increasing the instantaneous bandwidth of the system is accomplished by:

1. Adding an ADC board to each FE cartridge
2. Adding an LO for the new ADC boards
3. Adding a processor board
4. Adding an optical combiner between the new ADC boards and the new processor board

Adding an FE cartridge requires:

1. Adding a set of ADC boards that equals the number of ADC boards of the existing cartridges
2. Adding an LO connection to each new ADC board
3. Connecting the ADC boards to an unused input of optical combiners in order to connect the ADC to the processor board

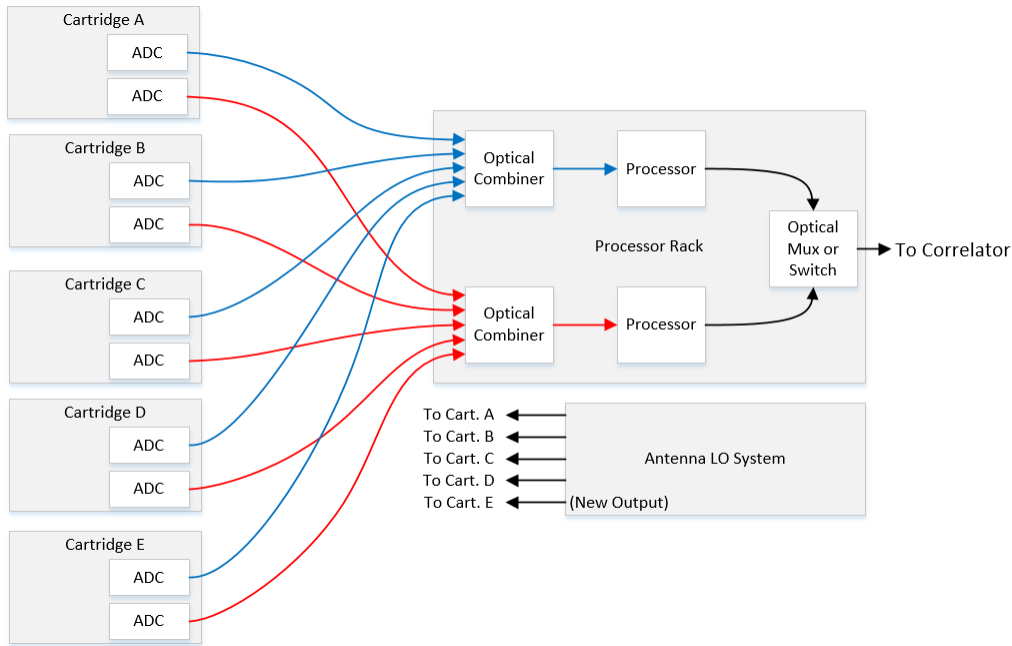


Figure 27: Possible signal transfer diagram.

The maximum number of cartridges and the maximum number of ADCs will need to be decided at the beginning of the design to determine the scale of the LO system and the number of inputs to each optical combiner, or the LO system and optical combiners should be designed to be replaced as the system scales up.

This design increases the modularity of the system and decreases the complexity of the RF section of the Digital Front End at the cost of increasing the number of ADCs. The FE RF switch that is in the current design has been replaced with ADCs on each FE cartridge and an optical mux for the digital signals from the ADCs. This increases the performance of the digital FE by removing a source of gain variation and RF noise from the system. The high bandwidth ADC designs allow this modular design to be feasible by reducing the number of ADCs required to cover the increase in bandwidth from each FE cartridge.

4.3.1 Cost estimate comparison for modular approach compared to existing analogue switch solution

Current ALMA solution employs the analogue switching of IF power from ALMA cartridges output to down converter/digitizer modules. Costs of current system implementation in year 2000 US dollars is approximately \$180k per antenna which breaks down as follows: \$45k per IFP * 2 IFP + \$20k per DTS * 4 DTS + \$10k, where IFP stands as if processor and DTS stands for Digital Transport System.

Assuming equivalent replacement for IF to fiber hardware: New system is \$25k for a processor board x 2 processor boards = \$50k/antenna. This is only part. This approach assumes, that each analogue output is supplied with its ADC board. For the current bandwidth of 4 GHz per analogue output, an AD 8 Bit ADC can be used in the second Nyquist band. Available dynamic range from 8ENOB allows connecting ADC directly to cartridge output. Costs of such ADC is estimated to be \$2.5k per unit without bulk production discount and may decrease to as low \$1k per ADC chip in the near future when the faster models with more dynamic range is available. Here we also assume that ADC board costs will be dominated by ADC, because Nyquist filter can be made part of the same printed circuit boards as well as necessary amplification will be achieved by an SMD mounted MMIC amplifiers which are available at costs of \$10-20 per amplifier chip. The total addition for 10 cartridges with 4 outputs each is $10 \times 4 \times 2.5 = \$100k$ while total cost for modular design with current capability would be \$150k with the tendency to decrease to just under \$100k per antenna. One of the major factor in the costs for analog switching is the costs of phase stable cables which can easily amount to \$500 per cable = total \$20k per antenna while cost of

optical fiber is negligible.

It should be recognized that the above costs comparison while clearly pointing in feasibility of modular solution even for baseline configuration has several oversimplifications and critical points:

- We compare costs of analogue switching/ADC of 15 years old technology with modern estimate of optical routing, without actually demanding processing power (IF bandwidth) increase.
- the costs of modular solution critically depends on ADC unit costs, which in turns depends on the bandwidth and amount of ENOBs required per analogue channel. While we are clearly at the break even for current ALMA bandwidth of 4 GHz per analogue channel, requirement of 8 or 16 GHz per channel will clearly prefer the analogue switching because there are much less ADC chips required while cost per ADC chip can be 10 times more.

Considering the above points, the most optimum modularity concept for current system may be a hybrid approach where a much simplified (can just be a coaxial relay with control) analogue switch is implemented in front of ADC board, followed up with processing board through optical link or with built in ADC, while a possibility to add extra ADC boards through additional optical link is maintained by allowing extra optical input channels. This will allow a customized cartridge solution to be added to the system without extra hardware costs, while maintaining baseline capabilities intact.

4.4 Digital Front-End functions

4.4.1 Digital Sideband Correction

In 2010 Morgan et al. [14] demonstrated a technique that would ease the manufacturing of 2SB receivers and increase dramatically its sideband rejection. In this approach the IF hybrid is removed, replaced by two Analog-to-Digital Converters (ADC), and implemented digitally within, e.g., a Field Programmable Gate Array (FPGA). The digital implementation of the IF hybrid allows to calibrate-out imbalances of the analog components allowing to achieve very high sideband rejections. The calibration of RF imbalances eases the requirements on phase flatness for RF hybrids and gain flatness for mixers and amplifiers, allowing the operation of 2SB receivers at frequencies and bandwidths where purely analog approach is impractical. During the last years this configuration has been implemented in receivers working at different RF ranges. The first implementation was demonstrated in a front-end operating at 4 GHz [15]. Later it was demonstrated in front-ends operating at the millimeter [16] and sub-millimeter range [17]. The same technique can also be applied to a fully assembled analog receiver [18], i.e. without removing the IF hybrid, improving its performance considerably. An average calibrated sideband rejection ratio (SBR) above 45 dB has been achieved.

The aforementioned results have the potential to improve the ALMA specifications on SBR from 7-10 dB (100%-80% of the band) to a much more desirable level of 20 to 30 dB. If implemented, the digital sideband correction system relaxes the requirements for the SBR level of the analog receiver substantially, enabling to reach at least an SBR of 30 dB with relatively simple hardware. This feature might be crucially important for future extra-wide IF and broad-band RF receivers for ALMA, where it is more difficult to make well balanced RF and IF components able to cover the required band.

4.4.1.1 Description of Digital Sideband Correction System

Digital sideband-separation systems have been successfully demonstrated for ALMA-type receivers based on SIS mixers [17][18]. The SBR level was demonstrated to be above 40 dB in the entire range of the receiver (figure 28) and only limited by the ENOB of the ADC board [18]. Figure 29 shows the general configuration of a 2SB receiver and the schematics of the digital configuration used to calibrate the system. The digital circuit can be placed either at the output of the mixers or at the output of the IF amplifiers. In the former case, the IF hybrid is actually implemented in the digital circuit. In the latter case, the calibration is applied to the full analogue receiver.

In the digital circuit used to calibrate a 2SB receiver, the outputs of the analogue part are digitized and combined with certain weights (complex coefficients) to suppress the image signal

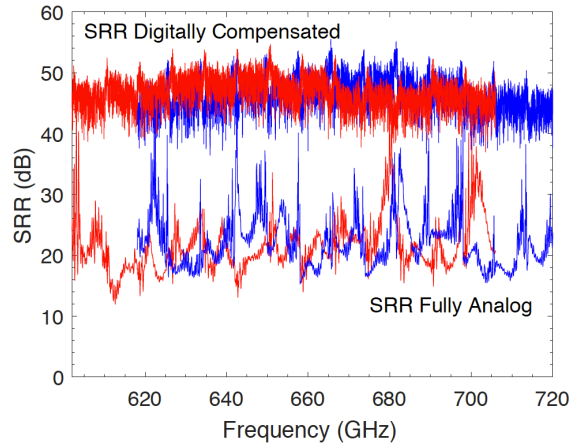


Figure 28: Comparison of the SBR obtained by analogue and digital means. Red and blue traces correspond to the LSB and USB frequencies, respectively.

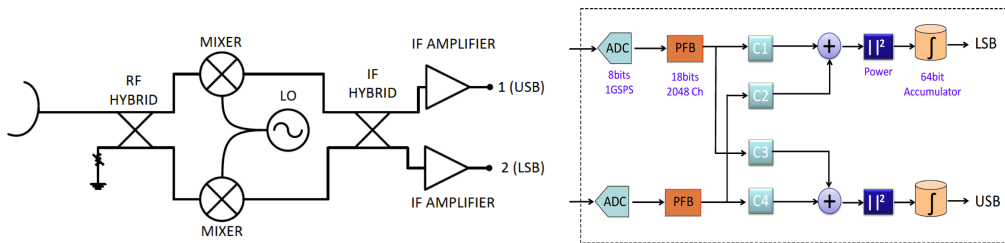


Figure 29: Schematics of an analogue 2SB receiver (left) and a digital extension for sideband correction (right). The digital extension can be used either with the IF hybrid or instead of it.

[18]. These coefficients are unique for each combination of LO and RF frequencies. They are calculated at an initial calibration measurement, where a CW signal (so called test tone) at the RF port is injected in the receiver and measured in both IF channels. Since this step is rather time consuming, the calibration is usually performed at a subset of LO and RF combinations which are, then, used for interpolation. An important practical question that needs to be addressed is how fine the frequency step of the test tone should be in order to provide accurate enough calibration, i.e., warranting an SBR level of 20 to 30 dB.

As mentioned above, the digital sideband correction can be used for analogue systems with or without the IF hybrid. A comparison of these two cases has been studied recently [18]. It has been concluded that in both cases, after correction, SBRs above 40 dB can be achieved. As an example, an analogue SBR of 22 dB was improved to 46 dB. Moreover, it was demonstrated that the analog receiver with an IF hybrid is more robust to some systematic errors [18]. Here "systematic errors" means the digital deviations relative to calibration, which are appearing in the system between the IF hybrid and the calibration board, for example unbalances originated in thermal drifting of the IF amplifiers or twisting of warm IF cables. As it is shown in [18]

4.4.1.2 Width of calibration channel for digital sideband correction ("first F" engine channel)

The calibration coefficients measured and used by digital sideband correction system can be perfectly valid only for a certain frequency of LO and RF, because they compensate for particular combination of RF and IF imbalances of current system. As soon as RF signal is shifted, the imbalances become different. The question is: how large can be the frequency offset from the original RF calibration frequency to guarantee still a certain SBR level. The answer on this question provides a very important practical number: the **maximum possible calibration channel width dW** , or a **channel width for the "first F" engine** of a FFX correlation scheme. Also, this parameter has a direct influence on a speed of calibration. The goal for SBR level is the following: 20dB guaranteed, and 30dB desirable, as it is formulated in proposed specifications.

It is clear, that the estimated calibration channel width is different for each type of 2SB receiver, i.e. it needs to be estimated separately for each existing ALMA band (2SB one) and for also for potential future instruments.

4.4.1.3 Experimental study of the channel width for the "First F" Engine

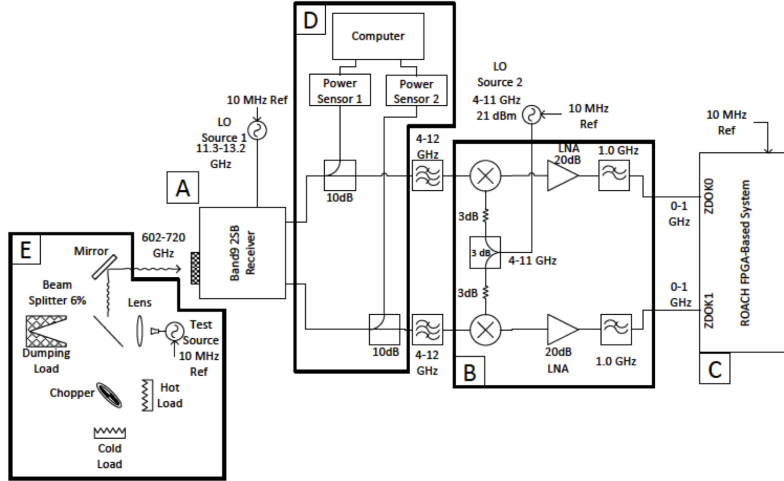


Figure 30: Schematics of experimental setup for demonstration of digital sideband correction system with 2SB receiver for ALMA Band 9.

The experimental analysis was performed for ALMA-type 2SB receiver cartridge for 600-720 GHz using calibration curves measured with high frequency resolution, measurement channel width is 244 KHz. The scheme of the setup is presented on Figure 30. In this case digital sideband correction system was used with the full 2SB receiver, i.e. IF hybrid is present. Results of analogue and digitally corrected SBR are shown above in figure 28.

The point of study is to find how much the SBR level degrades if one applies calibration numbers of a certain channel for the neighbor channels. This dependence was studied in statistical way for the the entire RF range. The results are presented in figure 31. Basically, the plots show that if we use a certain calibration for the channel of $64 \times 244 \text{ KHz} = 15.6 \text{ MHz}$ away, the SBR will be still guaranteed above 30 dB in entire RF range. From the right plot in figure 31 one can conclude that even 128 channel window (31.2 MHz) still gives SBR above 30 dB level. Based on that, the **"first F" engine channel width can be 62.4 MHz** assuming calibration in the middle of the channel. Important to mention, that this number is valid for this particular ALMA-type 2SB receiver cartridge for 600-720, which has IF cables length of 300 mm and isolators in IF chain.

4.4.1.4 Analytical Analysis of the channel width for the "First F" engine. Estimation for existing ALMA bands

The analytical analysis was based on assumption that RF imbalances are changing slowly with frequency, but the IF imbalance can change fast due to much lower frequency and because of shorter periods of standing waves caused by much longer connection lines between the IF elements (normally, between 200 mm and 350 mm for ALMA receivers). It means, the IF imbalances will be the limiting factor for the calibration channel width.

Firstly, the intrinsic imbalance of the IF hybrid was considered. The numbers, given by manufacturer shows imbalance as good as -30 dB [19][Band8]. In addition, this imbalance is changing very slowly with frequency, which corresponds to period as wide as few GHz.

Secondly, the imbalances generated by reflections from SIS mixers and IF isolator (or IF amplifier) were studied. The most critical reflections are shown on figure 32. Following the numbers: "1" is the intrinsic imbalance of the IF hybrid, "2" is a SIS-to-SIS leakage through the hybrid isolation, "3" is a amplifier-to-amplifier (or isolator-to-isolator) leakage through the hybrid isolation, "4" is a complex reflection from one of the amplifiers (isolators) and afterwards from the SIS mixers, which

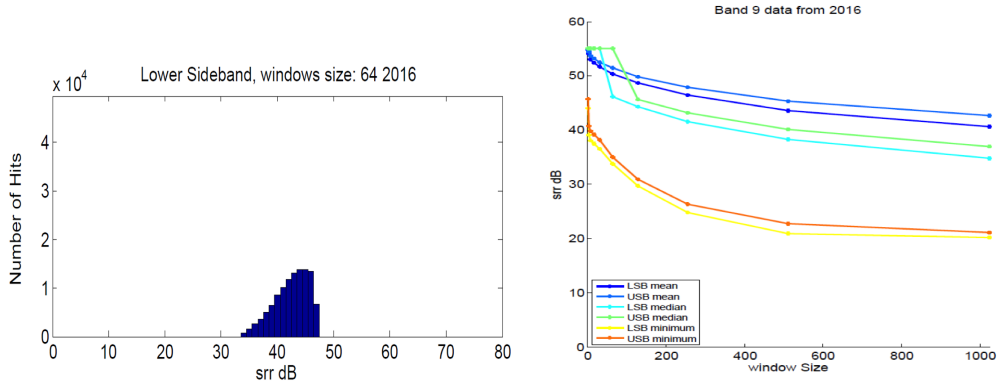


Figure 31: Left - Number of channels with certain SBR level for a calibration window width of 64 channels (15.6 MHz). Channels with SBR above ADC dynamic range (48dB) were discarded. Right - dependence of SBR level on the calibration channel width. . The most important are the yellow and the orange curves, which correspond to the extreme min level of SBR

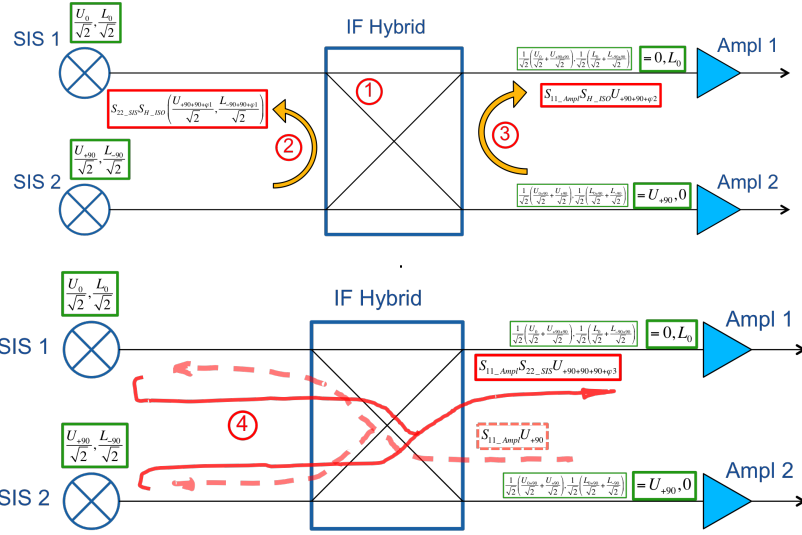


Figure 32: General diagram of IF part of 2SB SIS receiver demonstrating 4 largest reflections contributing to IF imbalance. In case the IF isolators are present, they should be put here instead of IF amplifiers.

is passing through the hybrid twice. The amplitude of generated imbalance can be estimated in the following way:

- for "1" imbalance is above **-30 dB**, non periodic
- for "2" imbalance is $S_{ISO}(Hybrid) * S_{22}(SIS) = (-25 \dots -30 \text{ dB}) + (-5 \dots -10 \text{ dB}) = -30 \dots -40 \text{ dB}$, periodic – period is determined by the cable length SIS1-Hybrid-SIS2. Here $S_{ISO}(Hybrid)$ is the isolation of the hybrid, $S_{22}(SIS)$ is a reflection from SIS mixer.
- for "3" imbalance is $S_{22}(Ampl/ISO) * S_{ISO}(Hybrid) = (-12 \dots -18 \text{ dB}) + (-25 \dots -30 \text{ dB}) = -37 \dots -48 \text{ dB}$, periodic – period is determined by the cable length Ampl1-Hybrid-Ampl2. Here $S_{22}(Ampl/ISO)$ is the return loss of the IF amplifier (isolator).
- for "4" imbalance is $S_{22}(Ampl/ISO) * S_{22}(SIS) = (-12 \dots -18 \text{ dB}) + (-5 \dots -10 \text{ dB}) = -17 \dots -28 \text{ dB}$, periodic – period is determined by the cable length SIS-Ampl times 2.

The outcome from derived numbers is the following: 1) the dominating imbalance is due to reflection from the IF amplifiers (isolators) and the SIS mixers (number "4") 2) the bottle neck is the SIS junction reflection, which can be as bad as -5 dB.

Based on the numbers derived for schemes in figure 32, the imbalance "4" is clearly dominating, and the others can be neglected for the moment to simplify the analysis. In this case, the SBR level degradation versus the frequency offset dF from the calibration point frequency can be described by formula

$$SBR_{cal.digital}(dF) = 10\text{Log}_{10} \left(\frac{1}{2A_{IF}\sin(\pi/T*dF)} \right)^2$$

, here A_{IF} is an amplitude calculated as a square root of IF imbalance given by $S_{22}(\text{Ampl}/\text{ISO}) * S_{22}(\text{SIS})$, T is a period of this imbalance determined from cable length between the SIS mixers and the IF amplifier/isolator. The illustration of this formula is shown in figure 33 for periode T of 1000 MHz and for three different levels of IF imbalance (-15 dB, -17 dB and -20 dB).

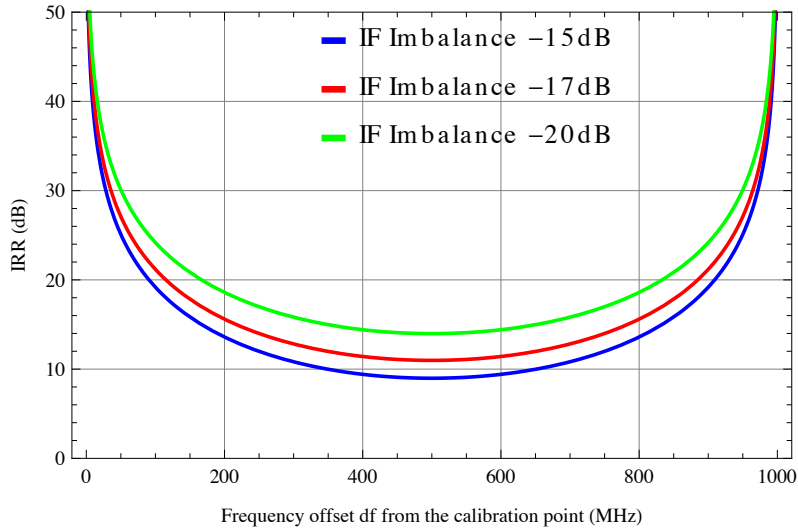


Figure 33: SBR degradation versus frequency offset from calibration point.

The frequency offsets, at which the curves in figure 33 cross the level of 20dB and 30dB gives the estimation for requested calibration channel width. Such a numbers were calculated for existing ALMA 2SB receivers and put in table 15. The calibration channel width or the width of the "first F" engine can be estimated as $2 * dF$, assuming that calibration is done in the middle of the channel. As example, to guarantee the sideband rejection ratio above 30dB for Band9 cartridge with isolators, one should have the "first F" engine calibration channel width below $30\text{dB } 23 \text{ MHz} * 2 = 46 \text{ MHz}$. This number is pretty close to 62.4 MHz estimated from experimental data for exactly the same system in the beginning of this section.

Table 15: Estimation of calibration channel width for existing ALMA receivers

	B3	B4	B5	B6(!)	B7	B8	B9* no isolator	B9* with isolator
Cable length (mm)	200	350	100	200	200(?)	250	250	300
T of reflection (MHz)	500	285	1000	500	500(?)	400	400	330
SIS S_{22} (dB)	5(?)	5(?)	5(?)	15(?)	5(?)	5(?)	5(?)	5(?)
S_{11} of isolator/amplifier (dB)	18	19	19	18	18	19	12	18
dF for SBR of 30 dB (MHz)	36	23	80	250	36	32	14	23
dF for SBR of 20 dB (MHz)	125	83	290	undef	125	116	46	82

(!) In Band 6 IF amplifiers are located after SIS mixers and before the IF hybrid. Due to very low S_{22} of the preamplifier, the reflection described in this table is not dominating probably, and the number in this table is not the best estimation for the Band 6 cartridge.

(?) SIS mixer reflection can vary a lot for different LO frequencies. Level of -5dB is rather realistic/pessimistic estimation

*The calibration channel width or the width of the "first F" engine can be estimated as $2 * dF$, assuming that calibration is done in the middle of the channel.

4.4.1.5 Calibration source. Calibration speed and stability

In general, the **source for SBR calibration** (SBR - sideband rejection ratio) can be the same as any standard test tone source used for SBR measurement by Kerr method [20]. The aim is to guarantee good enough signal to noise ratio in IF for the detected calibration signal. To get 30 dB rejection ratio one need more than 30 s/n ratio. Since only relative USB/LSB power is needed, the source signal does not have to be uniform for ALMA bands, nor the source should have a pure tone (comb signal is also good enough). The calibration tone power of few nW will be sufficient for any ALMA band. Here is the explanation of this estimation: if we take the SSB system noise temperature as 700K (worst case in Band 10) and channel width for calibration as 23 MHz, than $kTB = 1.38 * 10^{-23} * 700K * 23MHz < 10^{-13} \text{ W}$, or $10^{-4}nW$. I.e. with the test tone power of few nW we have at least 40dB of S/N. In the experiment with digital sideband correction for Band 9 2SB receiver, it was used a standard ALMA Band 9 local oscillator [18]. Because of too high power, this calibration signal was suppressed by tens of dB. Based on that knowledge we conclude, that a good calibration source for ALMA could be: 1) harmonic generator based on either a Schottky diode or on a superlattice diode [21], 2) photomixer [22]. The harmonic generator based on the superlattice diode was widely used in the lab as a test source for ALMA Band 9 beam pattern measurements, for characterisation of HIFI receivers, for beam pattern measurements at 625 GHz of SIS receiver for TELIS project [23]. A very effective harmonic generators based on Schottky mixers are commercially available in frequency range up to 170GHz [24] and availability for frequencies up to 950 GHz should not be a show-stopper, because Schottky mixers are known as effective harmonic generators even up to frequency of 3 THz [25].

Typical size of harmonic source is one cubic inch. It can placed on the ALMA robotic arm calibrator. The source is a zero-bias (or self-biasing) device, so for operation it needs only a microwave signal generator providing frequency about 15 GHz with power up to 15 dBm. Standard YIG-oscillator can be an option.

Stability of the callibration source is not critical, because the calibration dump cycle takes milliseconds. Relative source power USB/LSB is registered and compared with black body source power.

Time of calibration. The calibration for curves shown in figure 28 was done during about 2 hours with high frequency resolution step of 244 kHz. It means 120 GHz were covered with step of 244 kHz for about 7200 seconds (one point takes about 15 ms, which is limited by stabilisation time of the reference signal generator). In case the calibration would be done with wider step of 23 MHz (the smallest dF from Table 15), it would take only about 80 seconds to cover 120 GHz. As alternative, calibration can be done for each particular LO frequency just before the measurement. It means 8 GHz for current ALMA could be calibrated for about 6 seconds (200 frequency points for the test tone). Table 16 shows estimated time required for calibration in case of different possible calibration scenarios at ALMA. This estimation is done assuming calibration time of 15 ms per point and 23 MHz step. Depending on system stability, it will be possible to choose different calibration strategies: i) calibration for particular LO point just before observation; ii) calibration of required bands once a day; iii) others.

While stand alone sideband ratio calibration source is an attractive option due to high signal to noise that can readily achieved. It is possible to obtain phase and amplitude calibration coefficients for digital sideband separation by observing a bright wide band sky source with ALMA as an interferometer. Utilising Walsh switching, ALMA can derive corresponding coefficients both in phase and amplitude using cross correlation in main correlator. Achievable accuracy of these coefficients which will determine the ultimate digital sideband ratio needs to be evaluated taking ALMA system and observational parameters into account.

Table 16: Estimation of time, required for calibration of the digital sideband correction system

Case	Corresponding BW	Calibration time
Full IF for one LO point Current ALMA 2SB (IF 4-8 GHz)	4 GHz * 2 = 8 GHz	5.3 sec
Full IF for one LO point Future ALMA 2SB (IF 4-16 GHz)	12 GHz * 2 = 24 GHz	16 sec
Full RF for current ALMA Band 4 (125 - 163 GHz)	38 GHz	25 sec
Full RF for possible AMLA Band 10 2SB (787 - 950 GHz)	163 GHz	107 sec

4.4.1.6 Conclusion, 10 years perspective

- For 2SB receivers installed on ALMA (B3-B8) the "first F" engine channel width can be up to 46 MHz to provide 30 dB SBR level and it can be as large as 166 MHz to guarantee SBR of 20 dB.
- Thinking of possible upgrade of Band9 (without isolators), the "first F" engine channel width should be 28 MHz to provide 30 dB SBR level and 92 MHz to guarantee SBR of 20 dB.
- The "first F" engine channel width is mainly determined by IF chain: by reflections from SIS mixers, from Isolators(or amplifiers) and by the cable length between these elements.
- phasing/VLBI requirements drive the channel width to 32 MHz see section 7.5.1
- Results presented in Table 15 are the first order approximation, and for very accurate answer all four imbalances described above should be taken into account or the entire IF circuit should be simulated for each particular ALMA band.
- The "calibration channel width" can be used as a standard parameter for future upgrades of ALMA receivers.
- Digital sideband correction system makes easier future upgrade of receivers to wider RF range and wider IF bands (up to 20 GHz), because system relaxes the requirements for the SBR level at the cartridge level. As it is shown in [18] the new required IRR level can be as low as -3 dB to guarantee the digital SBR level above 20 dB. This level of -3dB can be considered as a potential new requirement.
- In general, if the IF hybrid is taken out, this will remove the limitation on \mathbf{dF} due to IF reflections, so the required \mathbf{dF} might be even wider. The trade-off is having a sideband ratio calibration more sensitive to drifts and errors appearing in cables between the receiver and the digitizer. To answer this question a separate study including tests in the lab and preferably at some telescope should be done.

Looking on the numbers presented in Table 15, it would be interesting to mention new approaches in design of compact sideband separating receivers. A very compact mixer was developed by researchers from IRAM (International Research Institute for Radio Astronomy, Grenoble, France) in papers [26],[27]. They demonstrated IF hybrid integrated in one assembly with SIS mixer. It makes distance between the SIS junction and the IF hybrid equal to several millimeters. Alas, it is not possible to put this receiver in the Table 15 based on publications, because the information about the IF hybrid S-parameters is not presented and the cable length between the IF hybrid and the isolator is difficult to estimate. Any way, assuming the most compact modification using this technology one could expect the "cable length" number to be as small as 50 mm (twice shorter than for the current Band 5). Assuming other components having similar performance, it would give the \mathbf{dF} of 160 MHz for SBR of 30 dB SBR and about 580 MHz for 20 dB.

In general, it is logical to expect an improvement of the 2SB SIS receiver technologies in direction of shorter cables, lower reflection from the SIS mixer and better S_{11} of the isolators. This expectations are highly probable if we would consider fixed IF range, but taking into account

high demand on serious extending of the IF band to 4-16 GHz (or even 6-18 GHz), it would be save to stay conservative and use existing number for future.

4.4.2 Base band equalization

A gain equalizer at the output of each channel is used, to ensure the signal to noise ratio requirement is met when the signal is re-quantized to 4 bits for data transmission. The digital processor board will channelize the data from the ADCs, and then provide gain equalization for each channel. Since the expected sample rate of each channel is expected to be low (≈ 8 MHz) compared to the FPGA clock rate(512 MHz), the DSP resources for the gain equalization can be shared between channels. With existing FE catridges, a 9 taps FIR filter seems to be sufficient to remove the ripple from any output channel having a bandwidth of 11 MHz or less, which is ripple seen in the current band 9. While decreasing the number of output channels will decrease the size and complexity of the polyphase filter bank slightly (see figure 35), it will greatly increase the DSP resources required to implement the gain equalizers. This is due to an 11 MHz ripple in band 9, which would require a significantly larger filter for the gain equalizer to remove the ripple as the bandwidth of each channel increases. This increase in size of the gain equalizer filter is due to the additional changes in gain vs frequency across the output bandwidth as more ripples are included in each output. In addition, the rate of change in gain vs frequency relative to channel bandwidth increases the size of the filter.

Since each gain equalizer is operating over a frequency range that is less than the ripples, each gain equalizer only has to remove the gain and slope from the signal in order to remove the majority of the effects of the ripple. If such a system was applied to the current ALMA side band, it would reduced the 5dB of ripple across the 8 GHz of bandwidth to less than 0.1 dB of ripple. The ALMA side band is shown in Figure 34, where the bandwidth of one 8MHz channel is less than the width of a pixel.

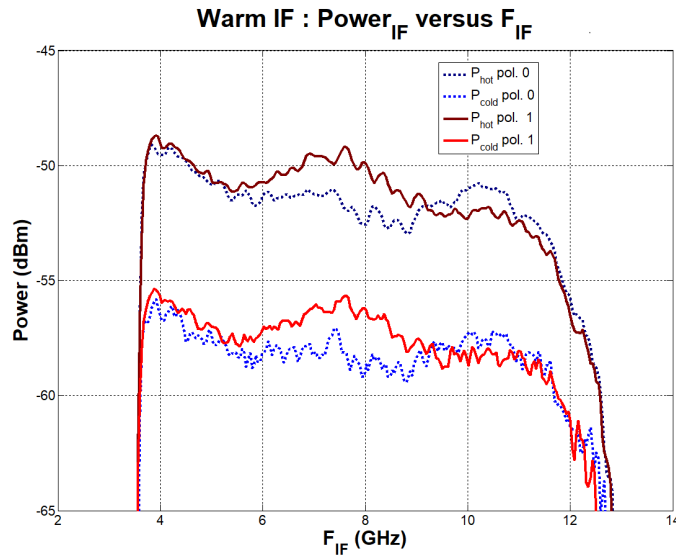


Figure 34: Example IF bandwidth of current ALMA system

DSP resources for a fixed filter size per channel do not change with the number of channels, since the data rate decreases as the number of channels increases, allowing for increased sharing of DSP resource. However, larger filters will require more resources, regardless of the number of channels.

If Digital Sideband Rejection is implemented, the base band equalization can be implemented with minor addition of digital resources. It requires an additional calibration step in which a hot load is used to to calculate the constants C1 to C4 (see figure 36) that equalize the IF band. Digital equalization is not different than analog equalization in the sense that, during observation, the pass band will be removed through on/off calibration. No data on the calibration constants needs to be transfer downstream, similarly as no data on analog equalizers is required to calibrate astronomical observations.

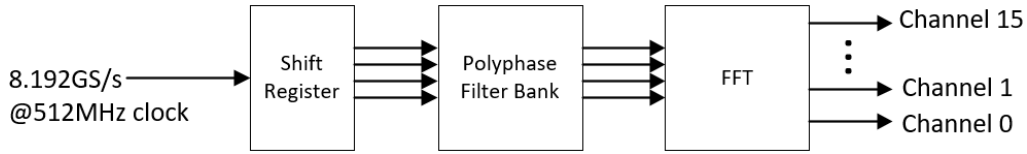


Figure 35: Polyphase Filter Bank

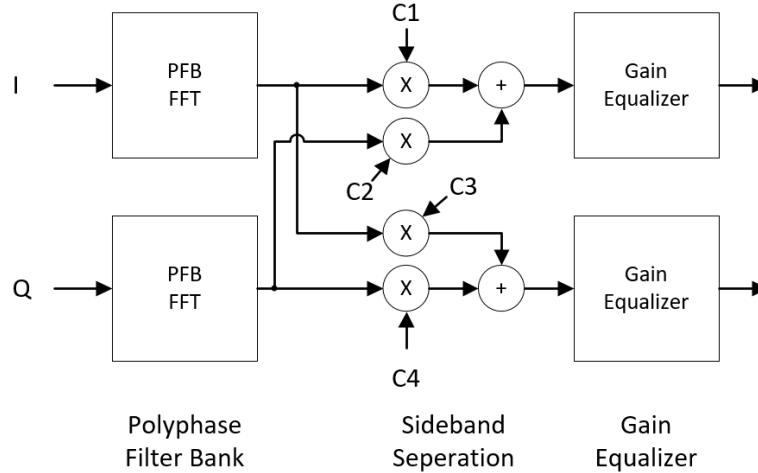


Figure 36: Scheme of digital sideband separation correction.

Since both digital base band equalization and digital sideband rejection is performed only once per receiver band tuning and calibration cycle, the calibration coefficients will be sent in ALMA main system without requiring significant increase of data transfer bandwidth in comparison with main data flow.

4.4.3 Interleaving ADC Spurious removal by adaptive filtering

While several methods exist to remove Interleaving ADC spurious, we give the scheme involving digital adaptive filters below as one of examples. Digital adaptive filters have been used to cancel Radio Frequency Interference (RFI), particularly in single dish radio telescopes operating in bands used for telecommunications. In this approach two channels (primary and reference) are sampled and any signal present in both channels is subtracted by the filter. The filter effectively cancels any RFI picked up by the main dish and by the reference antenna [28].

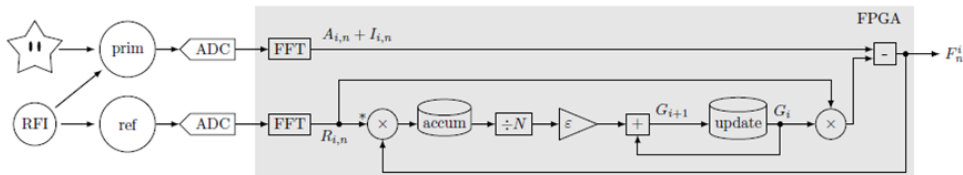


Figure 1: Schematic of the adaptive filter.

Figure 37: Adaptive Filter

Interleaving ADCs generate spurious signals due to the phase and amplitude imbalances between ADC cores. These spurious tones are coherent signals, in phase with the ADC clock. It has been noticed that when using the same type of ADC to sample the Primary and Reference channels, the ADC spurious are canceled, as if they were RFI picked by both primary and reference antennas.

The above result suggests that adaptive filters could be used to remove coherent ADC spurious allowing the use of many-cores interleaving ADC as samplers for ALMA. The reference channel can

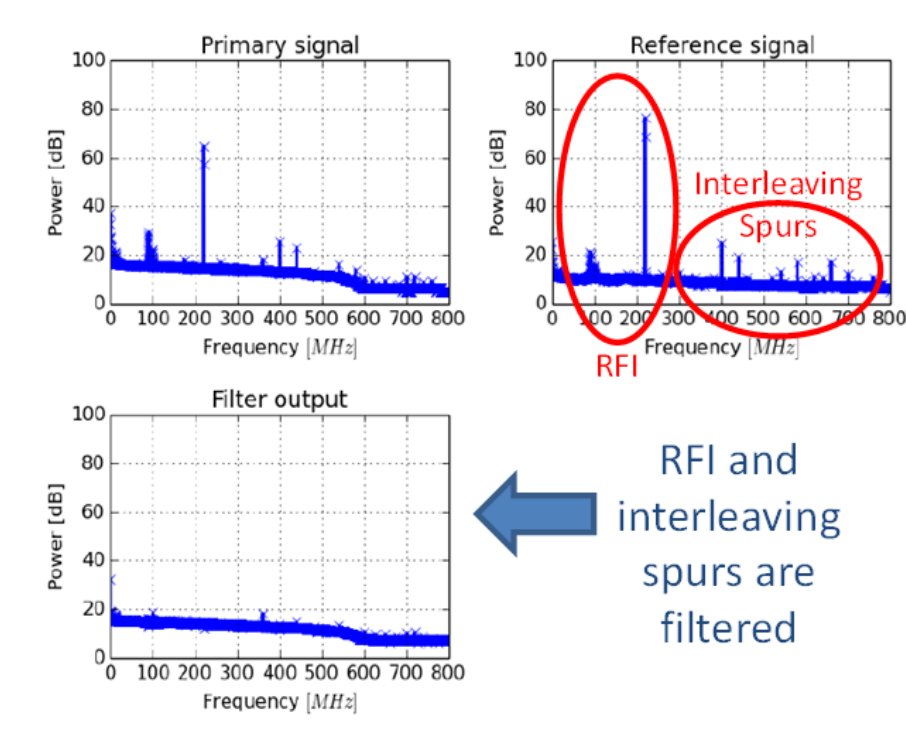


Figure 38: Spurious removal

be generated by an idle (loaded-input) ADC, or by a look-up-table designed to generate coherent tones in the frequency channels contaminated by the interleaving spurs. For the later application, no reference antenna is needed, since the reference signal would be generated with electronics in the antenna cabin or programmed into the FPGA.

4.4.4 Interfacing correlator (FX, XF)

High-speed Ethernet transceivers of 400Gb/s are about to come onto the market. This is over three times the current data rate for an ALMA antenna, per fiber. Using the 3 unused fibers in addition to the current DTX fiber from each antenna and lower overhead protocols, it is estimated that roughly fifteen times the current data rate can be transmitted from each antenna. Using lightweight data protocols on top of UDP will allow each channel of each processor board to have its own broadcast stream over a standard high-speed Ethernet networks. Care will be required to set up a network that can crossbar the larger data rates.

4.5 Digital platform (FPGA) including calculation power and projection

The digital platform will consist of multiple digital boards; each board will have an optical receiver, an FPGA, and a high-speed optical Ethernet transceiver. The optical receiver will receive the optical signals from an ADC board and convert the signal into electronic signals that will be received by the FPGA's high-speed transceivers. A modern large, DSP oriented FPGA will be able to process roughly 2 Tera-ops at less than 150 watts of power (find UltraScale_Plus_XPE_2018_2_2.xlsm power estimator spreadsheet using [29]). Ethernet interface chips, known as PHY chips, interface to higher lever processors through a protocol called media independent interfaces, known as MIIs. The MII is in standard IP libraries for FPGAs. Industry's multisource agreement for the 400Gb/s optical transceiver specifies a maximum of 15 watts of thermal dissipation. This means that each digital board in the digital platform will consume 155 to 165 watts.

4.6 Coarse F: digital channelization

The polyphase filter bank, shown in figure 35, is a resource efficient form of channelization, and can be implemented using the DSP elements common if modern FPGA families. In addition, the

high sample rates require the data to be transmitted to the FPGA through high speed transceivers, which create an array of samples that must be processed in parallel. To reduce the processing requirements of the gain equalizers on the output of each channel, the polyphase filter bank must create channel bandwidths less than the ripple seen in the worst case, which is the 11 MHz in band 9. This requires the polyphase filter bank to have 8 MHz channels, since the 8 MHz is the smallest power of two decimation of 8.192 GHz that is less than 11 MHz. The polyphase filter bank requires that the input samples be down-sampled into an parallel array equal to the number of output channels. Since it is desired to produce many narrow channels, the output of the high-speed transceivers must be converted to a wider parallel array at a slower clock rate in order to match the large number of channels.

A standard digital filter used in radio astronomy has less than 0.4 dB ripple over 90 % of the pass-band, has less than 3dB variation over 96 % of the pass-band, is down 10dB at 2 % past the pass-band cut off, and is down at least 40dB at 5% past the pass-band cut off. In practice, a polyphase filter bank requires a roughly 40 filter coefficients per output to meet these filter specifications. For a system that channelizes a 8192 MHz data stream into sixteen 512MHz channels requires 640 multipliers for the filtering and 256 multipliers for the FFT, or roughly 16% of the DSP elements in a Xilinx KU115 FPGA. A comparison of channelization processing requirements is shown in table 17.

The outputs of the polyphase filter bank have complex values, which means that re-quantizing the output for data transmission leads to changing the phase of each sample. Fortunately, due to the very small signal to noise ratio common in radio astronomy, the effect of re-quantizing complex valued signals is almost statistically identical to re-quantizing real valued signals. This means that the conversion from complex valued signals to real valued signals is unnecessary.

Table 17 shows the processing power required in terms of the number of multiplies per second. Since each DSP element contains a pre-adder and a post-adder with a multiplier, it is assumed that the limiting factor in the processing resources is the number of multipliers in the DSP elements. In addition, it is assumed that DSP resources can be share between subfilters and between output channels, so each DSP element performs many calculations per each output sample. The multiplications per second for the polyphase filter bank subfilters is the $c * i * s$, where c is number of coefficients per subfilter, i is the number of channels and s sample rate per channel. The multiplications per second for the FFT is $4 * i * \log_2(i) * s$. The factor of four is due to each complex multiply in the FFT requires four multiplications. The total DSP usage is the total number of multiplies per second divided by clock rate of the FPGA.

Channels	Output data rate per channel MS/s	Polyphase Filter Processing with 40 coefficients/subfilter (Gops)	FFT Proc. (Gops)	Total proc. (Gops)	Total DSP usage @512MHz	# of signals per KU115 FPGA @512MHz
16	512	327.68	131.072	458.752	896	6
32	256	327.68	163.84	491.52	960	5
64	128	327.68	196.608	524.29	1024	5
128	64	327.68	229.38	557.06	1088	5
256	32	327.68	262.14	589.82	1152	4
512	16	327.68	294.91	622.59	1216	4
1024	8	327.68	327.68	655.36	1280	4

Table 17: Processing requirements for channelization

5 Analogue processing and Digitization options

5.1 Analogue vs digital band switching

Current ALMA band selection employs analogue 10 position switch which communicates four analogue outputs of each cartridge WCA to a down converter. For 2SB cartridges, each analogue channel (4-8 GHz) is then split into two subbands (almost 4-6 GHz, and 6-8 GHz) which are down converted to a baseband 0-2 GHz. For DSB cartridges, which have only two analogue outputs of 4-12 GHz bandwidth, the signal is communicated to four downconverter modules and split into four base bands. Each base band is then followed by a 3 bit digitizer. This scheme has proven to work and is cost efficient when there are many expensive digitizers per analogue channels or there is an expensive analogue equalization board is required. When ADC would become increasingly broad band and higher dynamic range full digital/optical band switching as described in section 4.3 would become viable. This implies having one digitizer per any/or subset of unique IF outputs. Apart from apparent cost disadvantage digital band switching scheme has several key advantages:

- Each digitizer bandpass can be tailored to individual output conditions, such as analogue IF pass band ripple, IF pass band slope, by means of fixed adaptation. This simplifies analogue part as well as may lead to decrease requirement for dynamic range;
- part of future upgrade for multi band operations is already pre-paid, only more processing power will be required;
- processing part can be separated from digitizing part galvanically and also in distance leading to much less noise/spurious pick up;

Further trade offs will be discussed in detail in the trade off section (Section 8). One should notice that digital band selection is considered for proposed ngVLA instrument.

5.2 Analogue vs digital baseband equalization

Analog equalization can only be done before the ADC. There are analog gain equalizer chips on the market, like the HMC6545, that designed for high-speed differential digital signals on backplanes, but can be used in a single ended manner for frequencies of 0-30GHz. The HMC6545 has 9 taps, and is excellent at correcting slope and minor deviations in the band shape, but are insufficient to remove the ripple seen in many of the current ALMA IF bands. Digital baseband equalization makes use of the abundant DSP resources of the FPGA, and operate on a bandwidth smaller than the ripple seen in the ALMA IF bands. This means that a 9-tap filter is all that is needed to remove the slope and one second order feature in the baseband. While this would take 1024 9-tap filters, however, the low data rate means the DSP resources can share between filters. This means that the 1024 9-tap filters could be implemented with 180 multipliers operating at 400MHz.

5.3 ADC full band digitization, digitization, digitization options

In this Section, we first discuss in general terms and for broad IF ranges the compromise which is needed between high bit resolution and high clock rates to digitize broad band analog signals. Second, we present possible digitization schemes enabling to achieve high sampling rates and briefly discuss the main properties and testing of existing, fast analog-to-digital converters (ADCs). Some design options are proposed.

5.3.1 General considerations

ADCs use a finite number of bits, n , to represent the sampled input signal. Ideally, the value of n should be large to achieve a high quantization efficiency (a minimum of 5 to 6 bits is needed to reach 99% efficiency, see Figure 19). In practice, n must remain small enough so that the data rate does not become too high especially if the sampling rate, f_s , is high. High sampling rates (e.g. f_s above 2 GHz) are common in the mm/submm domain because broad band signals are required to improve either the signal to noise ratio (continuum observing mode) or the spectral line coverage and the line survey speeds. A compromise between the selected values of n and f_s is thus needed so that the digitizer delivers to the data processing chain a manageable bit rate, $n f_s$. In addition, a survey of the samplers available on the market shows that, independently of the used sampler

architecture, the effective number of bits tends to diminish as the sampling frequency increases. Therefore, selecting an n -bit digitizer with a high value of n may not be easy for high values of f_s . This selection is even more difficult if one wishes to achieve a high quantization efficiency and a high dynamic range so that the sampler can accept large signal variations across the broad IF range delivered by the front-end receivers.

Management of the current ALMA IF range requires oscillators for analog downconversion and bandpass digitization at a relatively low clock rate. Digitization at higher rates would simplify or could even get rid of the analog conversion stage thus improving reliability and calibration. However, it is difficult to design receivers without large signal variations or ripples across the current or future broader IF ranges. And only many-bit digitizers can preserve good statistics and a high dynamic range response while achieving a high quantization efficiency (see Table 14). But, as mentioned above, the need for a high value of n tends to ‘contradict’ the high value of f_s required to sample broad bandwidths. It is interesting to recall here that for the astronomical data analysis one needs to correlate spectral channels much narrower than the IF bandpass to be processed. Each individual channel (generated from the digital filtering system processing each antenna signal) is thus much less affected by ripples and 4-bit signal correlation, providing nearly 99% efficiency, is an excellent goal.

5.3.2 Current and future ALMA receiver IF ranges

The scientific community using ALMA has recommended to enhance the instantaneous bandwidth to improve the ALMA science productivity. The future 2SB receivers will provide outputs in at least the 4 to 12 GHz IF range. This will imply digitization of at least 8 GHz per sideband and polarization. The 4-12 GHz IF band has been indicated as a good compromise between wide IF and good receiver noise temperature [30]. The minimum noise temperature which can be achieved with cold low noise amplifiers increases with the maximum frequency to be amplified. This results in a trade-off between bandwidth and receiver noise temperature. However, recent work [31] suggests that the increase of instantaneous bandwidth beyond 8 GHz will greatly improve the continuum sensitivity even for a slight degradation of receiver noise temperature with IF bandwidth around 4-20 GHz. The slight degradation in receiver noise temperature would slightly degrade (a few percent) the spectral line observation sensitivity. On the other hand, a wide IF bandwidth would allow to speed up spectral surveys, especially at the higher frequencies of ALMA. From a technical point of view, two teams have already demonstrated good receiver performance with IF bandwidth in the range 4-20 GHz (i.e. 16 GHz per polarization per sideband) following two different approaches. At NAOJ, [32] have achieved a 3-19 GHz IF bandwidth by integrating a high-Jc SIS mixer together with a CLNA drop-in module in a single block. This approach will be investigated further in the future with the expected improvement of the bandwidth of commercially available CLNAs. At Harvard/Smithsonian [33] have been designed and tested a 4 - 22 GHz cold isolator to be used between the receiver SIS mixer and a CLNA in a conventional way. The same team plans to use this component for an extended 4-20 GHz IF bandwidth in the SMA. In addition, the European VLBI Network consortium is also studying receivers with an RF band from 1.5 to 15.5 GHz.

5.3.3 IF range digitization

As in the study on high speed digitization initiated for ESO by Univ. of Bordeaux, LAB in 2014, we consider here that either (i) single-rate or (ii) dual-rate digitization of the full IF range is possible.

(i) One may use either a single digitizer with an adequate high sampling rate or two interleaved digitizers in order to relax the high frequency clock requirement. These two single-rate digitization approaches are illustrated in figure 39 adopting the current ALMA IF range, 4 to 12 GHz, as an example (and without taking into consideration possible aliasing problems). In the first approach it is difficult to identify an adequate commercial device with enough bits whereas in the lower clock rate approach more bits could become available around 12 GHz. However, interleaving requires twice more devices than direct digitization and a specific calibration procedure is also needed.

(ii) A possible example of dual-rate digitization is shown in Figure 40 . The full bandwidth is digitized at relatively low clock rates but twice more devices than for direct sampling are needed. With such a scheme the complications related to interleaving clocks are not present anymore. However, the useful signal must be extracted from the two overlapping bandwidths that have been digitized; this requires signal processing in the FPGA that captures the ADC data.

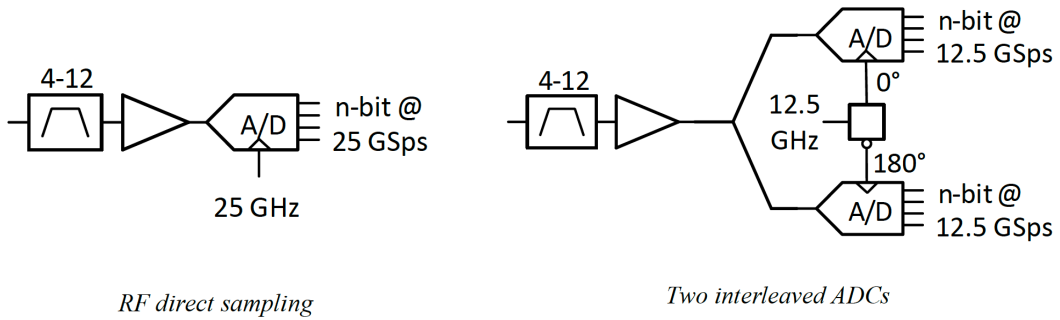


Figure 39: Basic designs for direct sampling of the 4 to 12 GHz IF range with a single ADC (left panel) and with two interleaved ADCs (right panel)

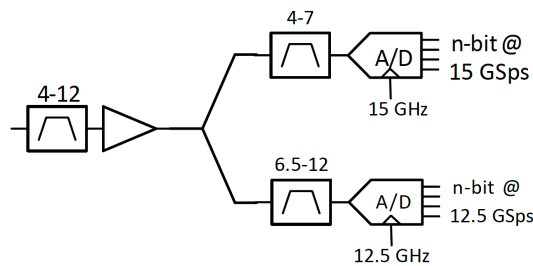


Figure 40: Basic design for dual-rate sampling of the 4 to 12 GHz IF range with two overlapping bandwidths.

Future SIS receiver developments will provide IF ranges broader than the 4 to 12 GHz considered above. We also note that for a next generation correlator, up to 16 GHz per sideband and polarization has been proposed in ALMA Memo 607 [34]. In this context, because the development of commercial fast samplers with many bits is slow and their availability somewhat unpredictable (see subsection below), one promising option to efficiently digitize broad bands seems to be dual rate digitization and interleaving of commercial samplers.

We have not considered here analog down-conversion as another digitization scheme because it uses mixers and tunable oscillators resulting in a relatively complex design and in more power dissipation than for direct digitization. However, this approach is used for the NOEMA interferometer with a digitizer clock around 8 GHz; but NOEMA only has 12 antennas while ALMA must equip 66 antennas and perhaps a few tens more in the future to improve sensitivity

5.3.4 Fastest COTS samplers.

The main simulated or measured properties relevant to this study for the fastest COTS samplers with more than 3-bit resolution are presented in Table 18. They could be useful for the basic designs discussed above and could eventually be proposed as the future ALMA digitizers.

Devices 1 to 5 can be purchased now, while devices 6 to 9 and 5+ are in progress. The three first devices have been developed with bipolar technologies which explain their relative high power consumption compared with the other devices designed with CMOS technologies.

The AC3401 device from Micram is a 2-way interleaved ADC and each core embeds a 1÷2 demultiplexing circuit.

The data outputs (12 lines per core after demultiplexing) are modulated with an internal pseudo random binary sequence (PRBS) circuit. This device was first tested at the company premises by the LAB team. The effective number of bits (ENOB) was above 4.5 across 4 to 12 GHz. The dissipation is relatively high, around 10 W. Core calibration took about 5 minutes. Later, the statistics from the 2 cores were examined and shown to be quite similar. In another test campaign performed at LAB, the earlier sampling frequency limit due to the FPGA used to capture the samples was overcome and the Micram device was operated up to 40 GSps with an ENOB above 4 bits. This demonstrates that the Micram device can digitize a 20 GHz receiver sideband in one

Table 18: Fastest samplers available from the market or in development

<i>N</i>	<i>Production company</i>	<i>Part number</i>	<i>Sample rate</i> ^{a),b)} <i>fs (GSps)</i>	<i>Resolution</i> <i>n (bits)</i> ^{c)}	<i>Input BW</i> <i>(GHz)</i>	<i>Power</i> <i>(W)</i>	<i>Cost</i> [*] <i>(€)</i>
1	Micram	ADC3401	34, &40**	6	20+	10	5.8k
2	Hittite-ADI	HMCAD5831	26	3.3	20	4.2	1.1 k
3	Adsanec	ASNT7123-KMA	16	4	20	4.3	1.1 k
4	Analog Devices (ADI)	AD9213	10.25	12	6.5	5.15	3.1 k
5	Texas Instruments	ADC12DJ3200 ADC12DJ5200	6.4 10.4	12 12	8 8	3 4	1.7 k (<3 k tbc)
6	Alphacore	Design in progress	25	4 & 6	~25	≤1	tbd
7	Pacific Microchip	Design in progress	20	6	~14	<1	2.5-4.5 k (tbc)
8	Pacific Microchip	Design in progress	56	8	>20	<1	2.5-4.5 k (tbc)
9	Teledyne-e2V	AQ900 (ADC concept)	>10.8	tbd	15-20	tbd	tbd

^{a)} The 20 GSps 5-b ADC from e2v (4 interleaved cores each at 5 GSps) used for NOEMA at 8 GSps is not included here because its production is discontinued; but see device number 9

^{b)} See text for IP macros enabling to reach about 60 GSps

^{c)} The ENOB for specific devices is given in text

* Approximate price per device assuming a minimum quantity of 100 units

** Device tested up to 40 GSps with ENOB > 4 bits, see text

go.

The HMCAD5831 ADC from Analog Devices-Hittite is a flash ADC design which has been evaluated by different teams. The LAB team performed both noise source and single sine wave testing. Good sampling behavior was observed up to 16 GSps and above but the ENOB was measured to be around 2.5. There is an over-range bit mode achieving 10-level operation which still needs to be tested. Without internal PRBS, the data capture may be problematic, limiting the maximum clock rate to about 20 GHz although higher rates are claimed to be possible with adequate air cooling and clock power. The dissipation is relatively low compared to the 10 W of the Micram ADC.

The latest fast ADC from Adsantec, ASN T7123, can be operated up to 16 GSps clock rate. It is a 4-b flash ADC with an internal PRBS. It has been tested at LAB and at NAOJ with relatively similar results for sine wave input signals. The measured ENOB reaches 3.1 to 3.3 up to 12 to 14 GSps. The 3-dB input bandwidth is about 12 GHz (measured at NAOJ). Digitization of a 3.9 GHz broad noise signal showed the expected band shape response.

The AD9213 from ADI (device number 4 in Table 18) can sample signals up to 10 GSps with low power consumption. The analog bandwidth is around 6.5 GHz. This design is based on an interleaved pipeline architecture. ADI might develop a 24 GSps ADC in a couple of years from now.

The ADC12DJ3200 from Texas Instruments (TI) (device number 5 in Table 18) can sample signals up to 6.4 GSps in single channel mode with low power consumption. The maximum sampling rate is much lower than for devices 1, 2 and 3 but the number of bits is definitely larger and the ENOB is expected to be around 8 to 9. The analog input bandwidth is around 8 GHz. This design is based on a folding and interpolating architecture. TI will introduce several new ADCs at the end of 2018. Two ADCs with sampling rates of above 10 GS/s and more are particularly interesting: A 12-bit ADC with integrated digital down converter (DDC) and an 8-bit ADC without DDC at a significantly lower price. Both ADCs (8- and 12-bit) will have an ENOB of 8 bit in the input frequency range up to 8 GHz. The dynamics of the new ADCs will also be excellent: SFDR is expected to be better than 55 dBFS.

The ADC architecture of the new TI high-speed ADCs is very similar to the ADC12DJ3200 (12-bit @ 6.4 GS/s). The ADC chip has 5 internal ADC cores; 4 ADCs cores are time-interleaved; the 5th unused ADC core is calibrated during this time and then used when another ADC core is re-calibrated. The method is called "background calibration" and we (MPIFR) have very good



Figure 41: Direct sampling for an IF range between 4 and 16 GHz, assuming that the ADC chip includes a demultiplexed output. The 4-16 GHz range is taken as an example and brings new science capabilities.

experience with this method with our FFT-Spectrometers (FFTS).

Texas Instruments will develop even faster ADCs in the near future. These high-speed ADC developments are driven in particular by new communication standards in mobile communication (e.g. 5G). Multi-bit ADCs up to 15 GS/s are expected in the next 2 to 3 years.

5.3.5 Design considerations for single- and dual-rate A-to-D conversion

In section 5.3.3 we have shown that there are basically two digitization options. One uses a single ADC for direct digitization while the other is based on dual-rate sampling to lower the clock rate at the expense of doubling the number of ADCs. In this section we explore the impact on the digitizer design of important new system and IF interface requirements assuming that we have a 4 to 16 GHz IF range. This range is in agreement with the new receiver requirement which calls for an IF range of at least 4-12 GHz with a goal of 4-20 GHz. The 4-16 GHz range is taken here as an example to investigate the technical constraints following from this choice while it would undoubtedly bring new science capabilities. (Our reasoning would be identical for 4-12 or 4-20 GHz IF ranges.)

5.3.5.1 Direct digitization

For the 4-16 GHz IF example considered here the clock rate is high and should reach at least 32 GHz which makes selection of an adequate ADC challenging. A sketch of the direct digitization option is shown in figure 41 and the provisional digitizer and IF technical budget are summarized in Table 19. According to Table 18 there are very few devices reaching this rate as of today. Therefore, interleaving two ADCs clocked at 16 GHz could also be considered although this would need twice more ADCs for the same total output rate.

There are several system and IF interface requirements to consider for a proper ADC selection. The IF interface requirements are mostly based on current ALMA experimental data. The most important requirements to consider here are:

1. Select a device with a high number of bits to comply with an overall efficiency (digitization and digital signal processing) > 96%;
2. Comply with power changes at the digitizer input up to 13 dB (dynamic range) ;
3. Achieve gain variations below 8 dB p-p across the baseband;
4. Provide enough gain for maximum and minimum in-band IF power levels -22 and -32 dBm.

Requirements 1) and 2): With 4-b re-quantization before correlation (98.8% efficiency), requirement 1) needs a minimum digitization efficiency of 97% so that an overall 96% efficiency is achieved in all circumstances. Figures 19 and 20 show that requirement 1) is met with an 'ideal' 4-b quantizer. However, as shown in Figure 21, the minimum 13 dB dynamic range, requirement 2), implies that 4 bits are insufficient to reach 97% efficiency simultaneously. Both requirements are met with effective 5-b, 6-b, etc. devices. In practice, a minimum of 6 bits must be implemented in the selected device so that a minimum of 5 effective bits are available.

Requirement 3): The simple relationship which exists between the signal power at two points in the passband, the ratio of the signal-to-noise ratio (SNR) at these two points and the digital efficiency allow us to estimate an SNR loss of about 5 or 2% for a passband slope of -6 or -3 dB assuming 97% efficiency. Similarly we derive that a power variation of 7 dB with respect to the nearby average power value would degrade the SNR by only 0.5 dB if 97% efficiency is met.

Table 19: Provisional digitizer and IF technical budget assuming an IF range of 4 to 16 GHz

Item	Value	Comment
Effective number of bits	5	Implemented bits >5 i.e. 6 bits or more
Max clock rate	32 GHz, 16 GHz	Direct digitization without interleaving. Interleaving doubles number of ADCs
Dynamic range at ADC input	13 dB	
ADC input level	0 to -5 dBm	Exact value depends on selected device.
IF range	4 to 16 GHz	Example investigated here. Long-term goal: 4 to 20 GHz
In-band ripple	8 dB p-p	
Max. and min. IF power level	-22 to -32 dBm	In-band value
Max IF gain	about 30 dB	

From these numbers we conclude that an effective 5-b device would efficiently mitigate an SNR loss across the passband due to slope variations or due to troughs in the passband.

Requirement 4): The minimum in-band power level requires sufficient IF gain to provide adequate input power to the ADC so that full scale operation is achieved. This depends of course on the selected ADC and its actual performance. If -3 to -5 dBm is needed at the ADC input stage then a maximum IF gain of order 30 dB is required.

Other design constraints: There are of course other constraints that must be taken into account for an actual design. We briefly comment here on aliasing. In the 32 GHz direct sampling case, aliasing may occur for signals above $32/2 = 16$ GHz in the 2nd Nyquist zone and beyond if there are spurious signals falling within and beyond the transition region of the adopted passband filter (steepness in the filter transition region is a key parameter). In addition, undesirable clock signal and system frequency harmonics could eventually impact the ADC outputs; they must be efficiently suppressed.

5.3.5.2 Dual-rate A-to-D conversion

Although direct digitization is a preferred option it is not a design specification and lower clock rate design options must also be considered. Dual-rate digitization is perhaps an interesting alternative even though we now need two ADCs. A possible schematic design is shown in figure 42 with two additional filters following the first 4 to 16 GHz passband filter.

The clock rates are 6 and 4 times the basic ALMA clock rate of the current system and lower than for the direct digitization option. Like for the direct digitization case above, the same technical budget considerations apply here but now for 24 and 16 GHz ADCs which potentially opens up the range of selectable ADCs. Table 18 shows that, at the present time, the 24 GHz rate is provided by the Hittite-ADI device, but with only 3 bits, or by the Micram ADC3401 device. However, in the latter case it would be recommended to use this ADC for direct digitization at its maximum rate. Other ADCs may of course become available in the near future as suggested by Table 18, so that we may have to select among a few different possibilities to reach the 24 GHz rate. (This clock rate could be somewhat lowered with a different combination of bandpass filters, 4 to 10 and 8 to 16 GHz for example with 20 and 16 GHz clocks.)

An FPGA card will capture the data delivered by the 24 and 16 GHz ADCs using the transceiver technology. Assuming for example 6-b digitization and a 1:2 demux stage implemented in each ADC we then have twice 12 outputs to be transmitted to the FPGA, each group of six toggling at 12 and 8 Gbit/s -whereas in the direct sampling case we have 12 outputs at 16 Gbit/s. One single large FPGA could process the same 8 GHz basebands (4-12 and 8-16 GHz) to deliver the original 4 to 16 GHz (or less bandwidth if that would be useful). The BP filter overlap shown here could of course be different depending on the selected filters and ADC clock rates. In the dual-rate option, bandpass overlapping eases the clock management; we also note that exact matching of the edges of two contiguous BP filters would be nearly impossible.

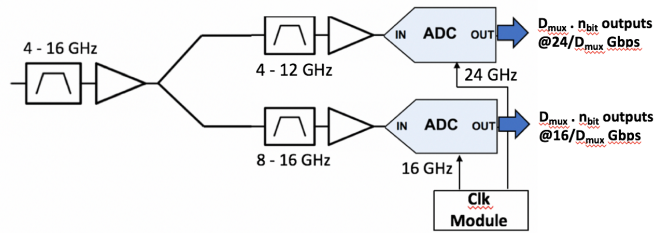


Figure 42: Dual-rate sampling for an IF range between 4 and 16 GHz, assuming that the ADC chip includes a demultiplexed output. The 4-16 GHz range is taken as an example and brings new science capabilities.

5.3.5.3 Further technical considerations related to high bit rate

Independently of the single or dual-rate design option, the need for a high effective number of bits requires to select ADCs with an ENOB of at least 5 bits which means in practice at least 6 bits implemented in the adopted device. We then have to transmit much more than the current 120 Gb/s sent to the ALMA fiber. Let us consider here that there is a 4-bit requantization stage in the FPGA that captures the ADC data so that the bit rate is lowered without impacting the overall efficiency of the 4-b correlator. Transmitting 32 GSample/s to capture a baseband of 4 to 16 GHz for all 4 outputs (USB, LSB and 2 polarizations) with 4 bits per sample and accounting for some margin due to fiber transmission protocol we need to carry a total of 640 Gb/s through the fiber. Wishing to use industrial and mature transceivers (TRX) compatible with span lengths above 16 km (baselines may be expanded in the future) we may use 20 or 40 GbE coherent transceivers (or even faster since industry standards are constantly evolving). This would require 32 or 16 TRXs per antenna and in fact twice these numbers with TRX modules usable at both ends of the fiber (data transmission to DWDM mux at the antenna and reception at DWDM demux before correlation).

Such a new design using industrial TRX technology and new DWDM will replace the demultiplexing chip following the current digitizer, transponders and DWDM used in the current system.

5.3.5.4 Brief comments on technology readiness and digitizer flexibility

The main challenge to implement a new single or dual-rate digitizer processing a broad IF (4 to 12 GHz and beyond) consists in identifying and qualifying an adequate fast sampler with a least 6 bits. Table 18 and considerations in section ‘Forward look to future high speed ADCs’ indicate that a mature ADC device meeting the new ALMA requirements is not yet available but that a few chips available now or still in development are promising although still subject to full qualification. The costs mentioned in Table 18 are provisional and may evolve.

On the other hand the TRX technology used to capture the fast ADC data is mature and allows us to design an optimal combination of ADC card and FPGA card to process the two sidebands and two polarization channels. In addition, new and rather cheap DWDMs are also available with as many as 160 channels.

There would be additional complexity if the new ADC design should be made backward compatible so that a narrower bandwidth could also be processed if that would be needed. Lowering the sampler clock rate should not raise any major difficulties. However, passband filters may have to be replaced.

Ideally, a new digitizer design should also be adaptable to an eventual future enhancement of the IF without changing the selected ADC. Very preliminary considerations suggest that this is achievable with new passband filters provided that higher clock rates are still a viable option. The latter condition seems more easily met with the dual-rate digitization option.

5.3.6 Forward look to future high speed ADCs

The University of Bordeaux, LAB team has developed contacts with Alphacore (devices number 6 in Table 18 with 4 and 6 bits) and, more recently, with Pacific Microchip (devices 7 and 8).

At the time of this report (Oct 2020) test samples from Alphacore have not been received by the Bordeaux group and it is not possible to anticipate if reliable chips will be available soon and if these chips could be modified to match the ALMA requirements. The Pacific Microchip ADCs are multi-cores and calibration for reliable ALMA operation could be time consuming and difficult. Despite these uncertainties the Alphacore and Pacific Microchip designs look promising. Other projects are under development by the LAB team including a new test campaign of the Micram products following the successful results obtained in 2019 up to 40 Gsps. Teledyne (formerly e2v) is studying an ADC concept (device number 9) for satellite communication applications. This ADC might be available in 3-4 years. (Teledyne had designed the 5-bit, 20 GSps, 4-/2-core sampler used by IRAM for NOEMA -see Note a) in Table 18.)

It is interesting to mention that IP macros interleaving many channels for ultra-fast ADCs (up to about 60 GSps with 8 to 10 bits) are available from Socionext (ex-Fujitsu with one Panasonic division) and Jarjet Technologies. The Socionext chip named CHAIS has been integrated in the Vadatech module (but with digital processing functions and memory not useful for an ALMA digitizer). These IPs are not packaged devices and would need high development costs to be integrated in digitizer modules. Jarjet Technologies offer an access program for customers for one of its IPs (dual 10-bit 64 GSps transceiver IC) for a \$2M NRE contribution. (Socionext offers a similar program for a similar price.)

We have listed in Table 18 state-of-the art or promising high speed ADCs. However, we feel that the development of a single core new ADC matching the future needs of ALMA (wideband IF ranges above 4-12 GHz together with robust operation and low power dissipation) will be slow. This is largely due to the fact that designing high speed ADCs is difficult with several design parameters function of one another (e.g. sampling rate, bandwidth, linearity or power dissipation). It is not clear either if the cost trends are favorable to the development of high speed devices using the thinnest processes. However, our plot of bit resolution versus sampling frequency (see Figure 47) and examination of our data base of commercial devices or ADCs in development with sampling frequencies above 500 MHz show, as expected, a loss of resolution with higher frequency (due to comparators ambiguity for example). This trend does not depend on the ADC selected architecture and suggests that 5- to 6-bit devices should become available up to about 50 GS/s in the future. However, it is highly uncertain to predict when such ADCs will become available and for which power dissipation.

In addition to the traditional digital electronics approach, in recent years, some new ideas have been proposed to design high-speed ADCs based on novel technologies such as non-linear transmission lines or photonic techniques (Kartner et al. 2012, Optics Express 4454). Such technologies are promising but still not mature or commercially available.

With the advent of 5G mobile data technology, many companies, which are active in the fast digital data processing domain, such as AD and XILINX are developing highly integrated high performance called RFSoc (Radio Frequency System on Chip). These contain high speed, high dynamic range (12, 14 bit DACs and ADCs) integrated with large high performance DSP, CPU and data transfer interfaces, such as 100 GBps Ethernet all integrated on one chip. This can offer very large space, power and cost advantages, especially when all NRE costs are already done as result of large investment in 5G program. This technology offers significant cost advantage in comparison of using discrete elements. Integration of components on one chip may compromise the stability and accuracy of digitization process and the feasibility of an application of RFSoc for a radio interferometer needs to be demonstrated.

5.3.7 Broad bandwidth digitization with many bits

Table 18 and testing fast ADCs indicate that providing many bits across broad bandwidths is difficult. The effective number of bits (ENOB) measured for a given clock rate with different input sine waves is always lower than the bit resolution. This lowers the design performance in terms of sensitivity (see Figure 19, efficiency for different bits versus threshold spacing) and further constrains the maximum ripple acceptable across the digitized IF range (see Table 14). The only two devices which offer a relatively high ENOB are the ADC12DJ3200 and the AD9213 samplers from TI and ADI, respectively. However, their maximum sample rate is 6.4 GHz for TI (or perhaps 8 GHz in the future) and 10 GHz for the ADI device. Their bandwidth is relatively limited compared to other designs. Nevertheless, Table 18 shows that a few ADCs would be convenient for dual-rate digitization or for single-rate digitization if we accept to interleave two ADCs. These approaches double the number of ADCs with respect to single rate digitization of the full IF range

with a single ADC. The latter scheme with more than 4 bits seems uncertain, however, especially if IF ranges go beyond 4 to 12 GHz.

The bit resolution versus sampling frequency trend mentioned in the previous section and the present status of the market suggest that $n > 4$ -bit devices should become available in a near future to digitize broad baseband 'chunks' but that it is still not appropriate to select a specific product. In addition, depending on the number of effective bits that we wish to adopt, external interleaving of two ADCs could also be considered.

5.3.8 Data transfer between high speed ADCs and FPGAs

Until a few years ago, data was transferred in parallel between ADCs and FPGAs. Because the data rate of GHz converters was often too fast for the FPGAs, the data streams were time-multiplexed. This led to a large number of connection lines between the ADC and the FPGA. Length matching of the lines was necessary so that the data streams could be transferred from the ADC to the FPGA without errors. Today's modern GHz ADCs from various companies offer a high-speed serial interface which is supported by FPGA IP cores and guarantees very simple data transfer from the ADC to the FPGA via a few connection lines. JESD 204B/C are standard protocols used by Analog Devices and Texas Instruments. Other protocols such as ESI stream, an open source data transmission protocol, has been adopted by Teledyne/e2v and Pacific Microchip. Moreover, instead of using electrical connections, the ADC data can be transmitted via optical modules and fibers. This makes it possible for the first time to separate the ADC and FPGA locally. Thanks to this "novel split architecture", the ADC can be placed close to the front-end and the FPGA a few meters away in another rack or cabin. The advantage of this new architecture is that home-made RFI introduced by the digital electronics are reduced. In addition, cooling of the ADC (close to the receiver) and of the FPGA board (in a separate rack) can be optimized. Furthermore, this modular approach allows the current ADC chip to be replaced with future better ADCs without changing the expensive FPGA boards.

5.4 Down-converter and high dynamic range digitization (multiple core ADC)

5.4.1 Down-converter

Digitization involving down-conversion is classically being used in the operational SMA and NOEMA interferometers as well as in the current ALMA. In the latter case the IF output is digitized using four 2 GHz wide down converter channels. The main challenge in current system is incomplete coverage of 4-8 GHz IF band which leads to inefficient observing spectral surveys.

In order to compensate for current ALMA system shortcomings and to facilitate DFE functions, requiring cross calculation of data in two analogue channels USB & LSB, we propose principle diagram shown in figure 43. The analogue signal from ALMA cartridge WCA (warm cartridge assembly) comes to variable gain wide band amplifier and then is split between down converter channels Band 1,2..n. Each down converter band has its own ADC, which can be any of the digitization solutions discussed in previous chapters. The output of ADC is then routed to an FPGA processing unit by means of serial data link protocol. Depending if FPGA processing unit is on the same board or separated from downconverter a copper based coaxial link or optical fiber link can be used. The latter opens possibility to place down converter module closer to front-end cartridge outputs. It also allows for potential integrate down converter boards in to cartridge and link it to processing board only through optical connection which transfers only already time labeled data packets. Naturally, the proposed scheme doubles elements for the related WCA output in order to perform cross calibration in the same FPGA unit. The amount of down converter bands and ADC's per down converter module depends on the balance between ADC's dynamic range and sampling speed and will be discussed in detail in trade-off section of this report. Today's technology allows for digitizer bandwidth of 5 GHz with 8 bits. Proposed scheme does allow bands of individual down converter modules to overlap, which makes it possible achieve *continuous band coverage* or use advance 2SB down converter schemes.

Main advantages of the proposed scheme are as follows:

- Continuous IF band coverage, without gaps
- Modular extension of IF bandwidth for future upgrades

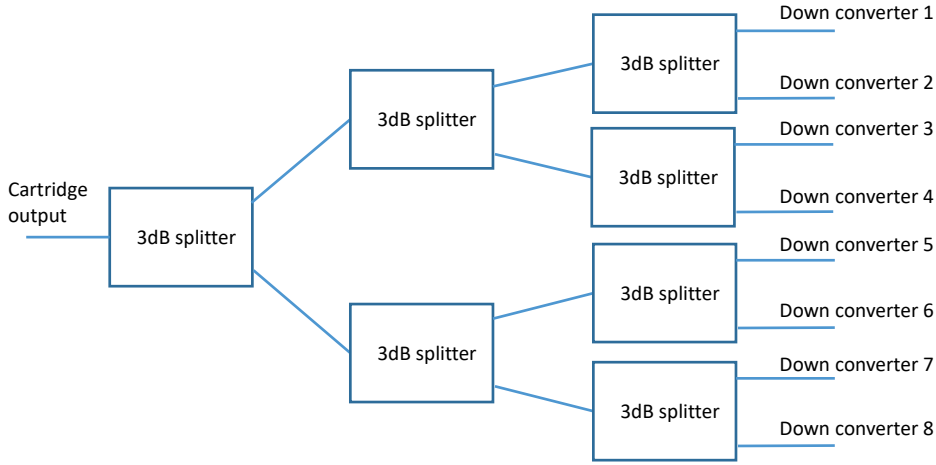


Figure 43: General down converter digitizing and data transfer scheme applicable to support DFE functions. Only WCA IF outputs are considered in the picture. Case for 8 outputs is shown as example. This 3dB splitter network can be realized on basis of PCB layout.

- Efficiently maps IF band onto digitization baseband for current ALMA ($f_{max}/f_{min} = 2$ or 3) utilizing full power of ADC
- provides additional flexibility through optical fiber link connection to processing board
- allows to extend current digitization bandwidth beyond one limited by ADC by employing several modules, which may allow also for single core ADCs

The disadvantages are:

- Large component count, compared with ADC only solution
- Possible increased level of spurious signal
- need of software loop to reduce spurious level

Typical example of IF band coverage by utilizing one or several down converter modules is shown in figure 44. For SSB down converter module, the band defining filter bandwidths can overlap and digitization bandwidth can be chosen to be wider than bandpass creating guard bands. This arrangement allows for continuous band coverage for multi module system as well as relaxes requirements both for band-pass as well as Nyquist low pass filter edges, simplifying the total system and making it more cost effective. The system bandwidth is then defined digitally in coarse F channelizer with channel to channel leakage as low as -80dB.

Both presented frequency coverage schemes has one major disadvantage, the LO2 (LO1 is main cartridge LO in our notation) signal from one module fall into the band of another module producing potential spurious signal, to be avoided according to ALMA specifications. One method to suppress this unwanted LO2 signal is presented in figure 45. The nominal signal path is from directional coupler C1 trough band pass filter BPF1 through directional couple C2, variable gain amplifier A1, mixer MX1, Nyquist low pass filter LPF2 and another variable gain amplifier A2 to an ADC chip. Output of ADC chip is converted to serial protocol and transmitted through optical/copper serial link to data processor. The LO2 signal originates in LO2 synthesizer, which should be shared between appropriate USB and LSB channel modules. It subsequently is split using directional coupler C3 into two paths: one directly goes to the mixer MIX1 and, another, which follows digitally controlled attenuator ATT1 and digitally controlled phase shifter PH1. Signal from PH1 is then coupled back into signal path using directional coupler C2. By varying coupled back

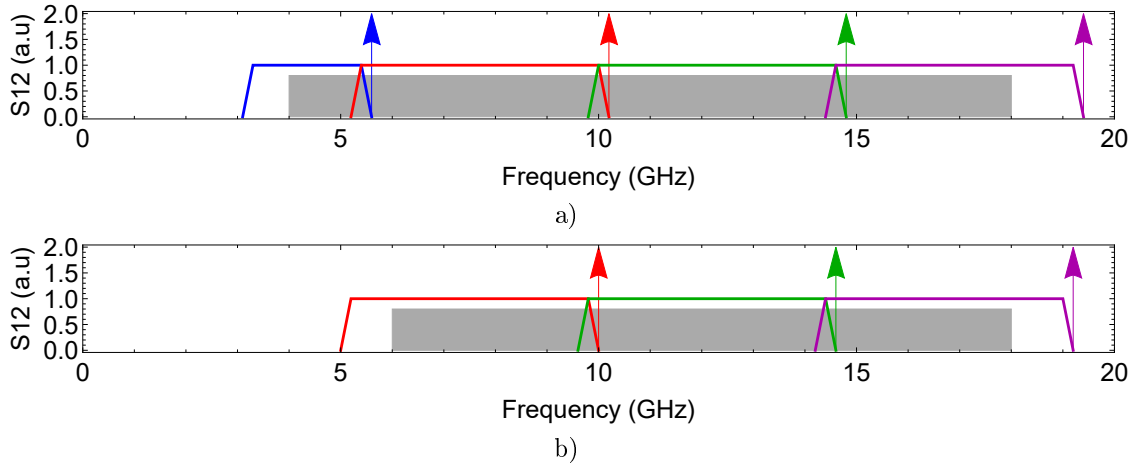


Figure 44: SSB down converter frequency plan and band coverage: a) in case that lower IF frequency is within the Nyquist band of main ADC and b) in case that lower OF frequency is outside of Nyquist band of main ADC. Gray rectangle represent main IF band, Band position of each module is shown in different colors and LO frequency is indicated by arrow. Main ADC clock rate is 10 GHz and guard bands are 0.2 MHz each side of Nyquist band.

signal amplitude and phase one can achieve nulling condition of LO2 leakage into the neighboring module. For the maximum suppression of -58 dB required, by specifications of #295.1 and #297 in table 3, phase regulation accuracy of 0.07 deg and amplitude regulation accuracy of 0.01 dB is required. This technique is commonly used to achieve pump compensation in superconducting parametric amplifiers. Higher orders harmonics of LO2 is effectively stopped by low pass filter LPF1 to an acceptable level. The higher order harmonics generated by the mixer are rejected by BPF1, which can be BPF + LPF in order to avoid spurious band pass of BPF at double/triple frequencies of a main band pass of BPF1.

5.4.2 High dynamic range digitization: multiple-core ADCs

Interleaving several ADC cores was briefly mentioned in section 5.3. Two-core ADCs are currently operated at the NOEMA interferometer (see footnote a) in Table 18) as well as at the SMA (at the lower 5 GHz clock rate) while we give in this section some details on the working systems developed at the MPIfR for single dish operations.

The MPIfR has been developing Fast Fourier Transform Spectrometers (FFTS) based on high-speed multi-bit ADCs and highly complex FPGA chips for more than 15 years. During this period of time the instantaneous bandwidth could be increased from 50 MHz (2003) to 4 GHz (2017) due to the availability of ever faster ADCs and more powerful FPGA's. Bandwidths up to 8 GHz are expected to be recorded and processed with future ADCs within 3 or 4 years. FFTS are now used in many modern observatories worldwide, e.g. APEX, SOFIA and IRAM 30-m. They have become a standard spectrometer in the mm and submm wavelength range. The FFT spectrometer has proven to be extremely reliable and robust, even under harsh environmental conditions, e.g. APEX at 5100-m.

FFT spectrometer uses high-speed time-interleaved multi-bit ADCs. Due to the relatively high dynamic range of these ADCs compared to previous one- and two-bit autocorrelation spectrometers, the demands on the IF band passes are relaxed. This has proven to be very important, because especially with wide IF bandwidths, it is often difficult to avoid a bandpass slope or even bandpass variations. With multi-bit ADCs, imperfect IF band passes can be corrected digitally in the FPGA before the bit width can be reduced to a few bits for further signal processing, e.g. correlation. In addition, high-dynamic range ADCs can improve receiver limitations. For example, it is possible and already demonstrated to digitally improve the sideband suppression or to digitally remove resonances or LO interference. Furthermore, possible ADC time-interleaving spikes can also be filtered out or calibrated out to an acceptable level using built in synthesizer module which provide test tone signal. These calibration periods are short (several seconds) and be done once a few hours, depending on thermal specifications of the environment.

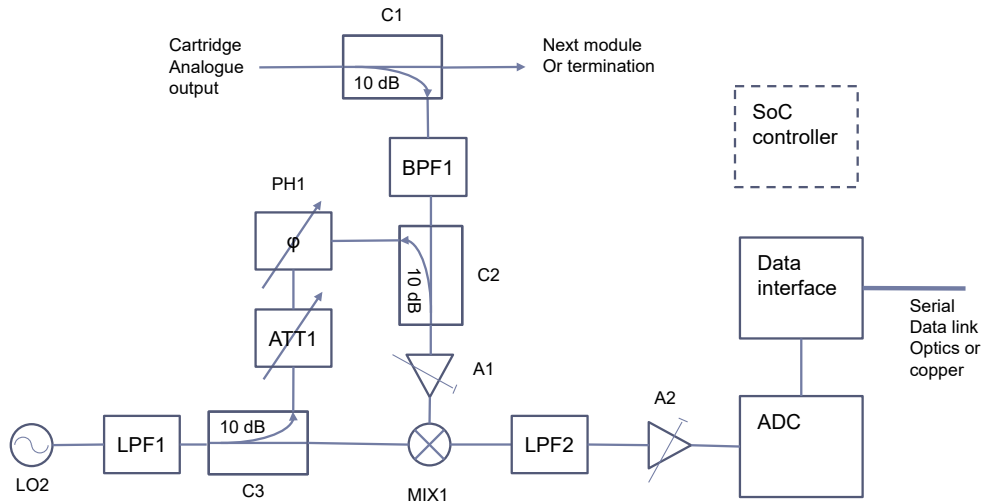


Figure 45: SSB down converter diagram including spurious compensation scheme. See text for explanation.

6 Digital transport system

6.1 Data transfer budgets

Each processor in the digital platform will receive 4 16GS/s data streams at 8 bits per sample (6.5 ENOB), or 512Gb/s from the ADCs, not including protocol data. Each processor will also transmit to the correlator the equivalent sample rate at 4 bits per second, or 256/s not including protocol data.

6.2 Data transport physical layer

One option is to use the DWDM 10 Gb/s transceivers which are currently being deployed in telecom systems. These transceivers can transmit data up to 80km at less than one watt. This would allow up to 96 10 Gb/s colors on a single fiber with standard telecom fiber optic equipment. Using the 3 spare fibers and the current DTS fiber from each antenna, this would allow up to 3.84Tb/s, or about 14 digital processor per antenna. The down side to this option is maintaining up to 364 transceivers per antenna on each side of the fiber. This comes to over 36000 transceivers for the main array and over 48000 transceivers when the compact array is included. Fortunately newer technologies are coming on to the market with faster data rates 100 Gb/s and still faster technologies are projected to be available by the time this system will reach construction.

The second option is to use the 400Gb/s transceiver technologies that are in development in industry. While this option reduces the total bandwidth in half compared to option one, one transceiver can transport the bandwidth of 1.5 processor board outputs. This means that using the same fibers as option one, 6 digital processor boards can transmit their data using 4 transceivers. This brings the total transceiver count to 400 for the main array and 528 when the compact array is included. The trend in data communication technology suggests that a transceiver will be able to reach two to six times the current data rate by 2025.

6.3 Trade offs

The number of transceivers in option one would make maintaining the data transmission system infeasible. While option two would not be able to transport as much data, the relatively small number of transceivers makes it a compelling choice. Given the rate that high bandwidth transceivers are improving, it is likely that a transceiver with twice the bandwidth or a transceiver that allows multiple transceivers to be optically multiplexed will be developed in the next five to ten years.

7 Distributed Correlator & Phased Array, and the DFE

The Digital Front-End (DFE) concept, the subject of this Study, requires digitization of received astronomical signals in the antenna. Proper control requires that the IF sampled time series be transformed into a coarse spectrum in the antennas and used in the DFE servo loop. The purpose of this section on the next generation ALMA correlator and phased array is to justify that the DFE, as here proposed, dovetails seamlessly with a next generation ALMA correlator and phased array concept. The latter proposal, in turn, is justified for inclusion on the ALMA 2030 road map on its own merits, independent of the DFE.

Our justification is based on the recent SAO-led in depth next generation ALMA Correlator and Phased Array Study whose final Closeout Report is published as ALMA Memo 607. The key architectural structures motivated are explained briefly. For in-depth details of the topics here discussed, the reader is referred to the referenced memo.

In bullet form the key technical alignments with the Digital Front-End are:

- A natural architecture for a wideband high resolution correlator phased array system is natively FX, rather than XF
- F-engine is divided into two stages to achieve the needed spectral resolution and to meet ALMA 2030 requirements
- It is advantageous, for processing efficiency, minimization of fiber payload, and technological reasons, apart from the needs of the DFE, to locate one of the F-stages in the antenna
- It is cost effective and natural to design the system in this way using industry-driven dense multiplexed Ethernet-over-fiber technology.
- Fast transmission of channelized data to the central signal processor, feeds seamlessly into the ultra-wideband Ethernet network needed also for the transpose or corner-turn from Station to Baseline-based domains.
- VLBI Beamforming is more easily implemented in an FX architecture, providing a suite of enabled science benefits, over and above supporting the DFE.

The subsections which follow justify these alignments between the proposed next generation correlator-beamformer architecture and the DFE here proposed.

7.1 The FX Architecture is superior to XF given current technology

Historically in radio interferometry, XF correlators—cross-correlation first, with Fourier transform in software on the integrated lags—have been favored because expensive wide multipliers are not needed. The bit-width of the multiplied data in the X-stage remains at the width of the sampled data throughout the processing. The advent of wide multipliers in digital signal processing hardware such as field programmable gate arrays (FPGAs) has effectively reduced the penalty for bit growth in the butterflies of the Fast Fourier Transform (FFT). The well known economy of the Cooley-Tukey FFT algorithm combines with the fact that correlation collapses to bin-wise cross-multiplication in the Fourier domain, to yield computational savings. Thus the number of instantiated multipliers for a given array size and spectral resolution is substantially reduced. Overall, given the width of multipliers is not a cost and complexity constraint, the the FX architecture allows for great economy in wideband correlators with high spectral resolution and relatively large numbers of antennas.

Also with wide multipliers, it is possible to process wider bit-widths, thereby improving the digital efficiency of the correlator from 88%, for a two bit machine, to 99% for 4-bits. This benefit which applies equally to spectral lines and continuum observations. The present ALMA correlator is limited to 3-bit sampled data. While it computes using 2-, 3- and 4-bit arithmetic depending on mode, the intrinsic efficiency is limited by the 3-bit samples. Further, the only modes being offered to ALMA users are limited to 2-bit arithmetic and 88% efficiency.

Sub-sample time delay compensation is required in interferometers to improve the loss of signal-to-noise ratio resulting from delay tracking errors. For XF correlators this can be accomplished in a dedicated circuit of the sampler clock sub-system by shifting the phase of the clock signal to the digitizers at each antenna, or by using a multi-tap adaptive Finite Impulse Response (FIR)

filter inline with the time series input stream. For FX correlators sub-sample delay compensation is simpler to implement by adding a linear phase increment on the output F stage at each antenna. This, compared to an XF architecture, reduces the hardware required in the DFE.

We consider the FX architecture to be compellingly justified in terms of computational and resource savings in a world where wide multipliers are an inexpensive resource. As an ancillary benefit we note in passing that the frequency response, spectral leakage, and dynamic range of FX correlators is improved over the XF. With the XF architecture correlation is performed over a finite time length before the FFT operation. This transforms to a sinc function in the frequency domain, the same response as a rectangular windowed FFT. With the FX architecture using a polyphase filter bank, the frequency profile provides a steep edge frequency response and low side lobe signals. XF correlators have fixed and high sidelobes of around -20dB due to the boxcar sampling of the X stage of the correlator. FX correlators have sidelobes of approximately -40dB, and these sidelobes are diminished down to less than -60dB with appropriate filter weights or use of the PFB prior to correlation.

For these reasons the FX architecture is now widely employed for modern digital correlators in radio astronomy [36],[37]. We further note that the current ALMA baseline correlator and ACA correlator adopted an FFX and FX architecture, respectively [38].

7.2 Two-stage channelization is required

Over the course of the referenced ALMA Correlator and Phased Array Design Study it was determined that two constraints, arising from assumptions and the scientific requirements, when combined drive the complexity of the F-engine architecture beyond reasonable implementation in a single stage. Briefly summarized these constraints are:

1. **Walsh switching:** to effectively demodulate the 90-270 Walsh pattern there must be an integer number of F-engine input sample windows within on Walsh step; ideally this would be a large number to avoid blanking losses. Additionally, this constraint drives non- 2^n transform sizes.
2. **1 kHz resolution:** the scientific requirement that the correlator provide a final resolution of ~ 1 kHz drives very large transform sizes which mean large input sample windows.

Given the immutability of the sample rate and Walsh step time, a single-mode F-engine implementation cannot reasonably meet both constraints as this would mean very large power-of-5 transforms with large input windows and unacceptable blanking losses; one constraint or the other must be relaxed. Therefore the Memo 607 Study [34] proposed the following two modes be implemented in the next generation ALMA correlator

1. **Walsh mode:** full Walsh switching³ is enabled but the ~ 1 kHz spectral resolution is increased to ~ 100 kHz, i.e. a relaxation of constraint 2. This would mean small blanking losses of $\sim 0.06\%$.
2. **LO-offset mode:** no Walsh switching. This mode incurs no blanking losses, and the window size can be large and a power-of-two.

These two modes naturally match the double-sideband (bands 9 and 10) and sideband-separating (bands 1-8) receivers, respectively, of ALMA. Should the upgraded wideband receivers in bands 9 and 10 be implemented with sideband separation (and it has been noted in review that this is contemplated) then this would considerably simplify the design of the correlator and its integration with the phased array, because the two distinct modes here discussed would not be required. In such an ALMA system LO-offset mode would suffice to improve cross-talk rejection and other imperfections. The substantial simplification due to the provision of sideband separating receivers across the full suite of ALMA bands would, in fact, be helpful in rendering the implementation of the next generation correlator in a simpler manner, and most likely at lower cost.

It should further be noted that the DFE depends for its operation on feedback of digitally derived spectral information from the correlator to downconverters in the front end. The Walsh switching (for sideband separation in a DSB receiver) or LO offset mode (to reject undesirable signal components) only serve to improve the measurement of the spectrum, and certainly don't degrade spectral design spectral resolution or similar. They are components of the system whose

³Full Walsh switching means both 0-180 for spurious signal rejection which is taken out with sign flips at the sampler and 90-270 for sideband separation which falls to the correlator

operation, otherwise, is orthogonal to that of the DFE, except insofar as they improve the DFE control through improvements to the measurement of the spectrum.

7.2.1 Architectures Studied

In the context of general algorithms for the F-engine the ALMA Correlator and Phased Array Study Team explored numerous architectures for the transform itself, including

1. Single-stage channelizer
2. PFB followed by per-channel DFT
3. Two-dimensional FFT/PFB
4. Prime Factor Algorithm FFT
5. Tunable Filterbank followed by per-channel PFB

These architectures were explored in the context of a set of assumed specifications listed in Memo 607 with estimated resource usage determined for a modern FPGA. Additionally, various other sub-systems relevant to the F-engine were investigated such as delay tracking and complex gain multiplication. The first option, which has only a single stage of channelization, was rejected as not being able to meet ALMA 2030 spectral resolution requirements, and the remaining options are various approaches to multi-stage channelization.

Figure 46 shows the last of the five considered F-engine personalities, which use a "Tunable Filter Bank" or TFB stage for high spectral resolution. Though this exact architecture was ultimately not favored, the block diagram shows enough relevant detail of the two stage channelization, and shows the complexity which is subsumed into the FPGA.

7.3 Location of first stage channelization in the antenna

There are a number of benefits to performing the first stage of channelization in the antenna. These benefits are over and above the need for antenna channelization to support the DFE with its attendant benefits. *A multi-stage channelizer in the correlator and phased array is absolutely required to meet ALMA 2030 requirements, and locating this stage in the antenna is a natural architecture. This is independent of the needs of the DFE, which further serves to reinforce the choice of multi-stage channelizer architecture.*

- The ability to perform gain equalization and digital sideband separation at a high bit depth prior to re-quantizing to the 4 or 6-bits per sample used in the data transmission system maximizes the effective bit depth at the correlator and therefore maximizes correlation efficiency.
- Performing the first F in the antenna also allows easier routing of the channels from the first F via standard Ethernet switches, as each channel can be routed individually to a selected processor block in the correlator.
- It is further possible to trim the guard bands in the in the frequency domain coherent data set, thus reducing the required payloads over Ethernet fiber.
- The most recent wideband analog-to-digital converters under consideration for the next generation ALMA system typically provide their data output on ultra-wideband asynchronous serial communications lines, which naturally interface to the asynchronous serializer-deserializer (SERDES) inputs on a current Field Programmable Gate Array (FPGA) family. The VCU118 evaluation board considered in the Memo 607 study provides twenty of these on a high density FPGA Mezzanine Connector Plus (HD FMC+) standard connector (VITA 57.3 standard⁴). The need to provide SERDES technology economically in the antenna leads to the probable need for, and provision of, an FPGA processor in the antenna, which in turn can be sized for a first stage of antenna-based processing.

⁴for more on this industry standard see <https://www.vita.com/>

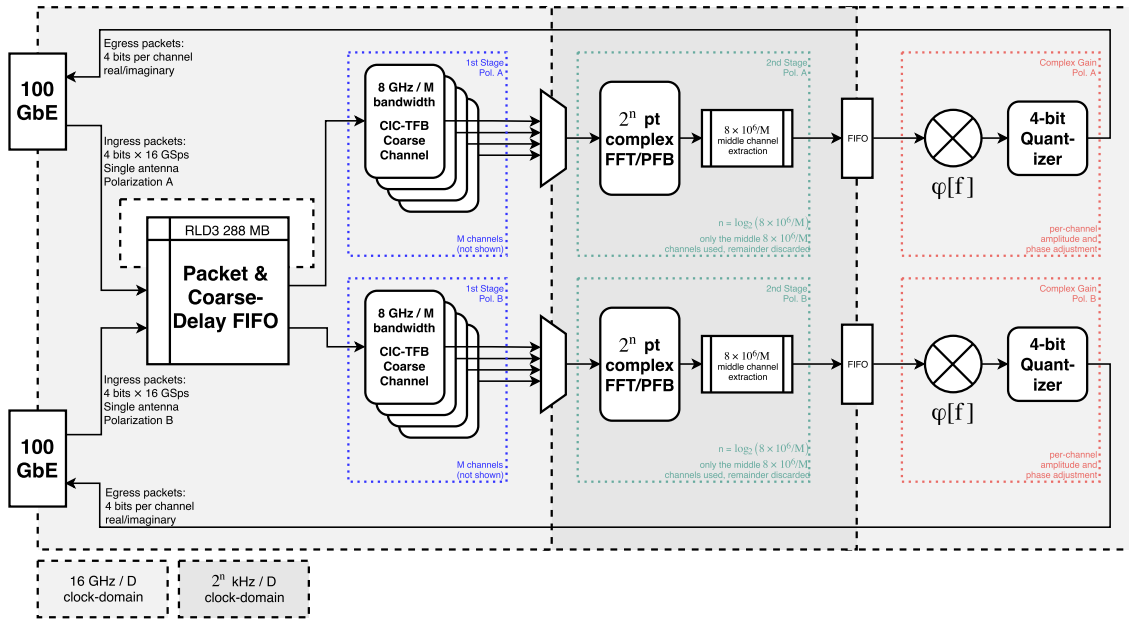


Figure 46: An example block diagram of a high spectral resolution candidate F-engine gateway personality that uses a TFB first stage channelizer followed by FFT or PFB (selectable) second stage fine channelization per coarse channel. This is an example of one of the multi-stage architectures studied in the referenced ALMA Memo 607. The incoming data packets contain 4-bit samples at 16 GSps; these packets are received with the 288 MB RLD3 modules available on the Xilinx Ultrascale Plus family VCU118 which is also used as a coarse geometric compensation FIFO. The data from each polarization is then fed to the first stage channelizer which contains a series of TFB channels each of which downconverts a sub-band of the full 8 GHz passband; note that the number of TFB channels, M , will generally be a low number, for example, 64, since the TFB logic scales linearly with M . Each TFB channel, containing $8 \text{ GHz}/M$ in usable bandwidth, is intentionally oversampled to the next power-of-two in kHz so that the proceeding second stage channelizer can be a power-of-two and the resulting fine channels are exactly 1 kHz wide. Ultimately the number of fine channels leaving the F-engine will be exactly 8 million but we’ve circumvented ever having to do a non-power-of-two transform. Note that only a single second stage channelizer needs to be instantiated since each TFB output is downsampled by a factor of M canceling out the fact that there are M coarse channels. Following fine channelization the complex gain sub-system provides per-channel complex gain multipliers which can be used to implement sub-sample delay adjustment, 90-270 deWashing, amplitude and phase bandpass corrections, etc. Finally the data is quantized back to 4-bits and shipped out to the BX-engines. Many subsystems needed for a full implementation are not shown, such as test vectors, monitor-&-control & (de)packetizers.

7.4 Networked corner turners and data transmission

All correlators require an interconnect system to allow communication between F-processing nodes, which operate on full-bandwidth data from a subset of antennas, and X-processing nodes, which operate on data from a relatively small bandwidth from all antennas. Since different ALMA base-band converters (BBCs) handling independent band fractions may be handled by entirely separate and independent correlators, the referenced ALMA Correlator and Phased Array Study has considered the implementation of a system for 72 dual-polarization antennas, capable of dealing with 16 GHz of processed bandwidth—8 GHz BBC bandwidth, two polarizations, and one sideband—and 4-bit samples. This amounts to 256 Gb/s per dual-polarization antenna (16GHz/polarization * 2 Polarizations * 2 samples per hertz (Nyquist sampling) * 4 bits/sample). Quadrupling this system covers the 64 GHz bandwidth of the complete proposed next generation ALMA system.

The DFE broadcasts each channel over ultra-fast Ethernet⁵ to a network of Ethernet switches

⁵The choice of speed will depend on what Ethernet technology is mature at construction time. 10 gigabit-per-second (Gb/s) has been used in the past, current experiments use 100 Gb/s, and it is anticipated that 400 Gb/s or even faster Ethernet technologies may be available when the design is frozen for construction.

that will allow any processing block in the correlator to listen to any channel from any antenna. The Ethernet switches replaces the crossbar switch in the current correlator. Each correlator processing block will use the timestamps in the Ethernet stream from the antenna channels to align the data for correlation.

7.5 FX Facilitates Beam forming and VLBI Recording

Beamforming the ALMA dishes creates a high sensitivity VLBI capability for ALMA that can be used to anchor centimeter, millimeter and submillimeter VLBI arrays for ultra-high angular resolution and sensitivity science applications. The Next Generation ALMA Correlator needs native beam forming capability that is expected to exceed the capability of the present ALMA Phasing System (APS). This new beamformer will enable VLBI and pulsar science at low and high frequencies and under a variety of atmospheric conditions.

7.5.1 Beam forming requirements

Beam forming for VLBI and pulsar applications imposes several specific requirements, some of which are necessarily dependent on the atmospheric conditions, array configuration and observing Band.

- Phasing efficiency of the antenna grouping in a coherent sum will be $> 95\%$
- Phasing of the array will be done as near to real-time as possible. This requires that either:
 - the target phasing efficiency can be achieved in an integration time short compared to the atmospheric coherence time on a calibrator source, *and* that system latencies are also short compared to atmospheric coherence, or
 - a buffer is used to store data so that phasing solutions can be applied to the data used in the solution.
- A real-time measure of phasing efficiency should be computed.
- Polarization leakage in the phase sum should be no greater than the average leakage for a single antenna.
- Data output of the phasing system should be available in standard VLBI format (2, or 4-bit data with suitable headers - e.g., VDIF).
- Multiple beams may be formed within the primary beam of the ALMA antennas
- Beams may be formed on sub-arrays of antennas and on sub-bands in frequency
- Phasing efficiency shall be as stable as the atmospheric coherence timescale
- Several modes of phasing should be implemented: phasing on in-beam target, phasing on in-beam calibrator, phasing on out-of-beam calibrator.
- Should be capable of correcting for source model and time variable atmospheric screen.
- Phasing should be available for all ALMA Bands.
- For the pulsar applications, the requirement is to be able to detect millisecond pulsars with a Dispersion Measure of 3000 pc cm^{-3} . This sets an upper limit on channelization of 32 MHz for ALMA Band 1. For pulsars, it is also desirable to maintain the maximum number of bits possible, but 2-bits are sufficient if any auto-leveling system has a time constant greater than ~ 5 seconds.

7.5.2 VLBI Recorder requirements

Modern VLBI recorders are essentially packet capture devices, that are currently capable of 16Gb/s. Packet headers, using the VDIF format, contain all the information required for routing of data in a VLBI correlator, including time-tagging. The VDIF format is expected to still be a standard for ALMA 2030.

It is possible that network appliances that are essentially just packet recorders—perhaps with Solid State Storage—could replace VLBI recorders. Capturing a single 64 GHz beam at 2-bits (256 Gb/s) could potentially be supported by extension of current VLBI recorder architectures, but to capture 4 beams, each 64 GHz bandwidth and 4-bits, the data rate would be 2048 Gb/s, for which a new generation of recorders would be required.

8 Overall trade offs and trends

In this section overall trade offs and trends for relevant technical solutions and technologies will be discussed. This discussion is **preliminary** and will be properly finalized in the final version of this document.

8.1 Digitizer trade off

Arguably, the most important trade-off discussion in this document is digitizer. First we summarize a minimum requirements for digitizer which follow up from relevant sections.

8.1.1 Key minimum requirements and their trends

Here we will summarize key minimum requirements for the system and their evolution of the time in order to aid the trade-off section.

8.1.1.1 Dynamic range

As discussed earlier, in order to simultaneously achieve 96% digital signal processing efficiency and at least 13 dB input signal dynamic range during an observation, an effective number of bits of at least 5 is required. Given the important contribution of other factors, such as system temperature and used bandwidth in the overall ALMA system efficiency, this minimum requirement will not evolve much over time. The ALMA gain variation across the full IF band is currently around 13 dB and the gain variation across baseband is even less. Therefore, selecting an ADC with 5 ENOB minimum, preferably 6 ENOB, will not deteriorate the input signal and, as mentioned above, this ENOB requirement is not expected to change in the future.

We note that accommodating power level changes between observations (due to first LO changes for a given receiver or to different receiver bands) with a fully digital high dynamic range system would require much more than 5 effective bits. We do not anticipate that such a system design would be feasible within the next 10 years.

8.1.1.2 Digitization bandwidth and analog channels

Current ALMA system digitizer bandwidth is 4 GHz per sideband with two sidebands and two polarization's. Current ALMA correlator supports this bandwidth only from two analog outputs resulting in total system bandwidth of 16 GHz. An upgrade for current correlator system which is currently in planning stage (TBC) will quadruple total bandwidth to 32 GHz (8 GHz x 4 IF channels) for year 2020 (TBC).⁶ Further increase of total bandwidth involves full upgrade/generation change of ALMA correlator or ALMA front-end. We foresee, that due to budget limitation ALMA front-end cartridges will remain mostly the same, with possible exception that band 2 and band 1 will support bandwidth of 8 GHz per IF channel. On the 10 years time scale we assume that either at least one more band can be upgraded to the 16 GHz IF bandwidth per IF channel or a double band observing may be introduced requiring twice the IF channels. We propose to have **16 GHz per output channel with 4 output channels with possible modular extension of both bandwidth and analogue channels** as minimum requirement, which would support dual polarization 2SB operation of one ALMA receiver band.

⁶As of August 2019, the correlator upgrade mentioned here has been cancelled

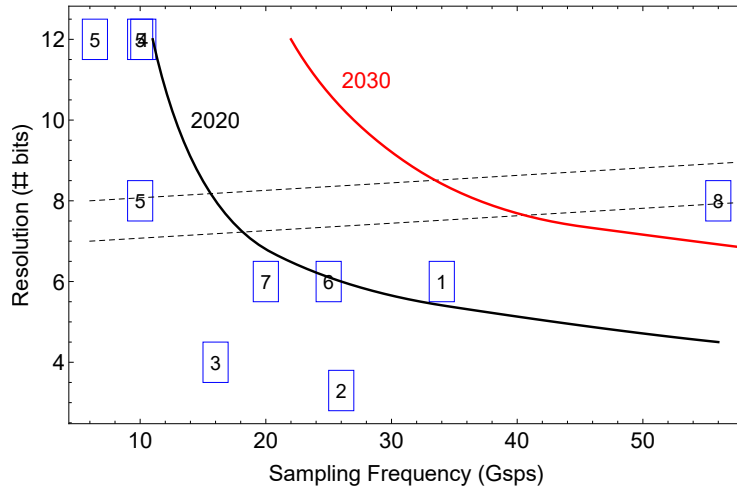


Figure 47: Trade off graph for sample rates vs ADC resolution. Current estimate is shown by the line "2020" and projection (TBC) is shown by the line labeled "2030". Numbers in labels correspond to row numbers in table 18.

8.1.2 ADC technology trade off

The most important technical trade off for ADC is sampling rate vs. dynamic range (resolution). Summary resolution vs sampling rate is shown in figure 47 which was based on information in table 18. Clear trend with larger resolution with lower sample rate can be observed. One should be careful considering resolution as pure criteria because real criteria is 6 ENOB system. There is natural trend in decreasing amount of ENOBs for the same resolution with increasing sample rate and ENOB is always less than resolution. This is indicated in the figure 47 as zone between dashed lines. Here we can conclude that there is only one ADC which can potentially satisfy direct digitization of 16 GHz base band or even direct digitization of 4-26 GHz band. However, this solution refers to study, relies only on one small company and actual ADC performance is not available yet. Most of higher volume manufactured ADCs from big companies follow the trend at the left of the figure 47. As it stands in time frame of 2019-20, a 4 GHz baseband with 20% guard bands can be digitized with 8 ENOBs using multi-core ADC solution with projection of 8 GHz in 5 years and 16 GHz in 10 years time frame.

Most of ADCs presented in figure 47 with resolution more than 6 bits contain more than one core interleaved internally. Calibration between cores proves crucial for spurious signal suppression. There is development of ADCs with advanced internal calibration procedures which shows good results in FFTS cores and needs to be investigated for the case of interferometer. The multi-core ADCs will naturally achieve much better resolution for a given bandwidth and if spurious signals will be brought under control this would be a preferred solution. One should mention a two core solution as one which has tolerable level of spurious signal.

The red line in the figure 47 is a guesstimate based on the following arguments. The mainstream ADC development will be driven by the most voluminous application in terms of amount of money and number of units. By far the biggest application is data processing for 5G cell network standard. Previous generation 4G + smart phone development led to much increased availability of compact on-chip RF components, such as synthesizers on chip, amplifiers, filters, down converters etc in the range of <2.8 GHz. The 5G RF band is much higher: range 1 - < 5 GHz and range 2 - 26.5...40 GHz, and so on up to 200 GHz. The first implementation of 5G will be range 1 and range 2. It will drive the demand to RF components range to be extended typically up to 5 GHz and up to 40 GHz, which is already happening now with, for instance, introduction of high frequency synthesizer on chip (AD9213) working up to 32 GHz. It becomes especially attractive to digitize the entire <5GHz band and do the processing all in digital domain for ground call infrastructure. The same, but later is likely to occur for 5G band 2, where, there will be first demand to digitize all available bandwidth of 14.5 GHz. Since 5G is oriented on high speed data transfer, it is important to notice, that maximum supported total data rate will be combination of bandwidth, which is fixed by regulations, and dynamic range (ENOBs) for a given digitizing system. This will create large demand/investment for a large dynamic range (amount of ENOBs) of ADCs in the 0..14.5 GHz

Nyquist band. This will lead to substantial effort and funds towards development of high dynamic range ADCs with large sample rates, in sampling speed of order of 30 GSPS. In fact, dynamic range needed for 5G is much more than ALMA requirement of 4.5 ENOBs. While there will be a demand for mainstream high rate/high dynamic range ADC through 5G development, there are physical limits for the switching speed of main technological components on which the ADC and further digital processing is built on. Likewise in computer CPU market, a raw increase of clock frequency has stalled and most of the increase in performance of computing systems is now achieved through parallel processing employing multiple physical processing cores. The same tendency for the same reason will likely be observed with ADCs: multiple core high ENOB ADC with intelligent calibration methods will be more common. Thus we predict there will be no change in the shape of the red curve in the figure 47.

8.1.3 System digitizer solution trade off

Each IF band of 4 analogue channels needs to be digitized. Depending on ADC speed achievable for minimum 5.6 ENOBs equivalent resolution, the IF band can be covered at once, using dual data rate solution. Due to high dynamic range requirements, there are no single ADC solution currently capable of digitizing whole 4-16 GHz band at once. A compromise can be made using the least amount of cores – two. Two core ADC produces relatively small amount of spurious and can be calibrated easier than its multiple core counterpart at the same clock rate. If ADC speed is not sufficient for required IF band, a down converter scheme should be considered in combination with above mentioned ADC solutions to cover the baseband. It must be noted, since down converter base band is smaller than highest IF frequency, we will consider a single unit down converter, because it can lower the ADC speed requirement for IF band at once coverage. We will consider relative weight of the following options and their reference labels in the following table 8.1.3:

- Full band dual core ADC without down converter
- Dual Rate Digitizer without down converter
- Down converter with dual core ADC
- Narrow band down converter with multi-core ADCs

These options have been preliminary evaluated ability to cover the largest bandwidth, ability to achieve required resolution in ENOBs, dissipated power, possible price factor, complexity factor, multiplexing ability, technical risk. Each field is evaluated applying score, the higher the better and scores are added to each other with same weight to form the final score column. When particular ALMA 4-12 GHz IF band is considered at this moment of time the dual band ADC will be preferred option because it exactly matches 1:3 IF coverage and possible to achieve with commercial devices. Parametric cost trade off is required in order to clearly distinguish further between direct digitizing and down converter options.

Architecture (ADC/ Down converter/...)	Full Band ADC	Dual Band ADC	Down conv. Full Band ADC	Down conv. Multi core ADC
Bandwidth	+	++	+++	+++
ENOBs	+	+	++	+++
Power Consumption, W	++	+	+	+
Cost	++	+	++	+
Complexity	+++	+++	++	+
Modularity	+	+	+++	+++
Technical Maturity	++	+	+	+
Spurious	+++	+++	++	+
Availability	+	+	+	+++
Score, flat ranking, # +	16	14	16	17

Table 20: Main trade offs for different digitization system solutions, assuming projection for year 2020

The main results of trade off considerations are present in table 8.1.3. The score in table is expressed in "+", "++", "+++" where "+++" is more "positive" score. The total ranking is obtained by equal weighting the coefficients, i.e. by counting total amount of "+". Each parameter in the table is considered as independent and ranked at the condition of all other parameters correspond to the system with equal specifications. The score considerations are given below for each line subject in the table 8.1.3

8.1.3.1 Bandwidth

Bandwidth or sampling rate is major consideration for all of the solution. Here in particular we consider achievable system bandwidth, rather than bandwidth per ADC chip. It is recognized that achieving larger bandwidth with a single ADC for required is the most technically difficult, so we expect full-band single ADC to have the smallest bandwidth, dual band ADC one step larger, down converted full band ADC even larger and modular downconverter with multi core ADCs is, technically, the largest because downconverter modules can be stacked to each other for practically any bandwidth.

8.1.3.2 ENOBs or dynamic range

Similarly to bandwidth, dynamic range is more difficult to achieve with single ADC, equally difficult to achieve with dual band scheme since the same single ADC is involved, while bandwidth advantage allows to have higher dynamic range (lower core frequency) for down converted full band ADC. For down converted multi-core ADC high dynamic range is the main advantage.

8.1.3.3 Power consumption

While power consumption per chip does satisfy the interface requirement with wide margin for all considered solution, the single chip ADC will be always more efficient for that criteria since it has only single set power conditioning components on board.

8.1.3.4 Cost

Cost contribution of downconverter module has been discussed in section 8.8.2. Main conclusion from there is that additional cost due to LO, amplifier, rf mixer and filters is well within \$600 per module. With this relatively low cost, the main criteria for cost factor is cost per 1GHz bandwidth for a particular ADC solution. While full band digitizer requires only one multiple core ADC, the cost per 1 GHz bandwidth is \$600 per GHz while AD 5 GHz bandwidth ADC has \$620 per GHz and AD 3 GHz chip has \$670 per GHz. Cost per GHz seems to be constant as a function of Nyquist bandwidth of ADC and is large with respect to the rest of component's cost. Therefore, system cost for all the solutions is practically the same with the margin of knowledge of ADC chip costs. Systems, utilizing larger fraction of their Nyquist bandwidth are preferred. This explains nearly the same cost ranking for all the solutions.

8.1.3.5 System Complexity

While systems considered has monotonically increasing amount of elements (left to right in the table), it is not only element count that describe system complexity. In addition a clock rate itself can be considered as system complexity as it is much more difficult to deal with at higher frequency. For clock rate the system has opposite trend. Therefore the seemingly very different system are scored closer to each other than if based on element count only.

8.1.3.6 Modularity

Under this criteria we consider that system can inherently allow to increase the bandwidth by adding modules of similar architecture to analogue output. This would be needed in case of a future upgrades or adaptation of the system. Both dual band ADC and dual band ADC has poor modularity as the system can not be extended without significant re manufacturing. The downconverter system have naturally high modularity as discussed in section 4.3.

8.1.3.7 Technical maturity

This field reflects if the chosen concept has been utilized by an interferometer before and has been successfully demonstrated. In addition, prospects of demonstrated successful operation are weighted in, for example, the downconverted multiple core solution calibration has not been demonstrated to work within interferometer system. This explains its lower ranking.

8.1.3.8 Spurious signals susceptibility

This field ranks potential of the system to generate spurious signals by its principle of operation. It is clear that down converted multicore solution will have the most spurious bands and the most demanding to calibration the spurious out. On the contrast full band ADC has minimum amount of spurious signals generated in the system.

8.1.3.9 Availability

This field reflects the fact, that very high rate ADC are typically developed by a smaller companies which have tendency to be more vulnerable to changing environment as well as have more risk to abandon production lines. That is why full band ADC (Adsantech) is scored lower than mainstream multi-core AD solution.

8.1.3.10 Total ranking and conclusion

Total ranking with equal weight of all discussed criteria does not reveal a clear cut optimal solution. Technical advantages and disadvantages of all solution balance each other and key cost factor does not have significant difference for solution discussed. However, there are several unknown technical factors that still need to be studied before solution can be chosen. First factor is ability to calibrate out spurious response due to multi-core ADC synchronization. Second important factor is the ability to calibrate out spurious signals from down converter LO's.

8.2 Analogue vs. digital DFE signal distribution from cartridges

This trade-off has been discussed in section 4.3. Although the digital signal distribution is more advanced is clearly more expensive. Trade off will be made in terms of price feasibility.

8.3 Analogue vs. digital equalization

As discussed in section 5.2, there is no viable and affordable analogue equalizer option which allows to alleviate significantly 6ENOB dynamic range requirements.

8.4 Analogue vs. digital sideband rejection

To reach 20dB of sideband rejection, the accumulated (RF hybrid + mixers + IF hybrid) imbalance between I/Q channels should not exceed 1.25dB in amplitude nor 8 degrees in phase, for all LOs and IF frequencies. These goals are very difficult to meet. The problem is in complexity of 2SB receiver, which causes multiple reflections in both RF and IF chains, and all of them contribute in total imbalance [39, 6]. The only way to have small enough imbalance is to minimize all of

these reflections, i.e. all the components should be top quality. This requires additional effort and attention to:

- machining with very high accuracy (in the order of a few microns, especially at high frequencies), the use of custom made tools, and lot of expert-technician time.
- mixer chips pairing, to ensure very similar performance, i.e. either manufacturing process should be perfectly reproducible, or a lot of mixers should be tested individually before pairing, which is time-consuming procedure.

Even considering all the care described above, and the relatively relaxed ALMA specification on sideband rejection (7/10dB for the 100/80% of the band), the yield of 2SB mixer blocks meeting specs was relatively low, and even after selecting the best mixers to be integrated into receiver cartridges, waivers for sideband rejection of delivered cartridges were not uncommon. As example, for Band 5 it was 22 waivers on sideband rejection parameters, each of them required additional effort to tune the mixers and roughly doubled the time for cartridge qualification.

The use of digital sideband rejection would ease the manufacturing of 2SB receivers considerably:

- chip-matching might not be required any more
- tolerances on RF hybrid fabrication will be reduced
- cryogenic isolators can be removed
- cryogenic IF hybrid specifications can be relaxed, making it much cheaper to manufacture
- furthermore, the option IF hybrid can be also considered.

All that allows significant reduction in size, complexity and cost for new cartridges.

If digital sideband rejection is available in the front end, for future ALMA cartridge manufacturers it will be an option not to provide 2SB receivers, but only IQ receivers (or low rejection 2SB receivers), so all the effort to achieve very high sideband rejection could be trade-off for bandwidth, noise and/or cost.

In addition, as it is shown in section "Digital correction of phase/amplitude imbalance" the utilisation of digital SBR correction system should improve observation time of current ALMA by at least 2%. If we estimate that new receives for ALMA can have 3 dB better SBR than existing ones, this number will be twice less, i.e. 1%.

Digital sideband separation processing needs no additional digital hardware with respect to currently proposed -FX- architecture, but the cost of implementing the calibration source, and the cost (in time) related to calibration overheads, as well as stability of calibration, need to be further evaluated.

8.5 Data transfer trade off

Data transfer trade off has been discussed in section 6.3. The main conclusion is, that with rapid development of standard TCP/IP data transfer over optical cable. A low overhead UDP switched optical data transfer system already will satisfy minimum requirement. The trend of increasing data rate will continue for years to come and will outperform the trend ALMA capability development, which will be investment limited. It is recommended to switch over from current proprietary data transfer, utilized in ALMA, to much more flexible standard TCP/IP protocol.

8.6 “First F” engine

Table 21 below shows briefly comparison of possible solutions for the “First F” engine. Due to bandwidth and space requirements in the antenna, FPGA and ASIC technologies are by far the best options to be considered.

Table 21: trade off table for different processing technologies

Type	Speed	Size	Bandwidth	Power/ calculation	Upgrade/ Update
CPU	slow	bulky	Low	High	easy
GPU	fast	bulky	Low	Medium	easy
ASIC	fast	compact	High	Very Low	hard
FPGA	fast	compact	High	Low	easy

The current correlator chips cost \$50 per chip plus a \$3M per production run. Using this as a reference we can compare the costs of implementing the first F engine using FPGAs and ASICs. The trade off FPGA vs ASIC capabilities is illustrated below:

FPGA vs ASIC

- FPGA (Development, One or two processors per antenna)
- ASIC (Lower power, Lower build cost if more than two processors per antenna)
- IF Moore's law holds:
 - The price of an equivalent FPGA may drop from \$12k to about \$750 by 2025
 - Lower FPGA prices means ASICs costs will be competitive at >65 processors per antenna

Current FPGAs:

- Kintex 7 Ultrascale (5520 DSP; 768MHz in datasheet; \$12k/chip)
- Stratix 10 (11520 DSP; 1GHz in datasheet; \$40k/chip)

The combination of compact size, low power, high bandwidth, and upgradability makes FPGAs the best choice for performing the first F in the antenna. Current analysis suggests we can put 5 polyphase filter banks in one Kintex 7 Ultrascale FPGA. To be conservative given that we wish to add some other DSP in addition to the polyphase filter banks, it seems it is possible to get 4 in a single FPGA. The processing power trend for DSP in an FPGA is 40% increase per year (see Figure 48), suggesting a 29 times increase in DSP power by 2026. This estimate will likely be on the high side, since transistor size is approaching quantum limits. Manufacturers suggest that the next generation of FPGAs will be based on 7nm or larger transistors, which would be a factor of 4 increase in processing power. While the total amount of logic may follow Moores Law, the recent trend in specialized FPGA families suggests that there way be families of FPGA with a increased DSP elements inleu of increased logic resources. Following Moore's Law would suggest we can increase the ADC channels in a single FPGA to 116, while a more conservate estimate would be between 16 and 32 channels. We may choose to improve the filtering requirements if we don't have enough ADCs or bandwidth to the FPGA for that many ADCs.

In conclusion, as for data rate there is clear preference for using FPGA technology.

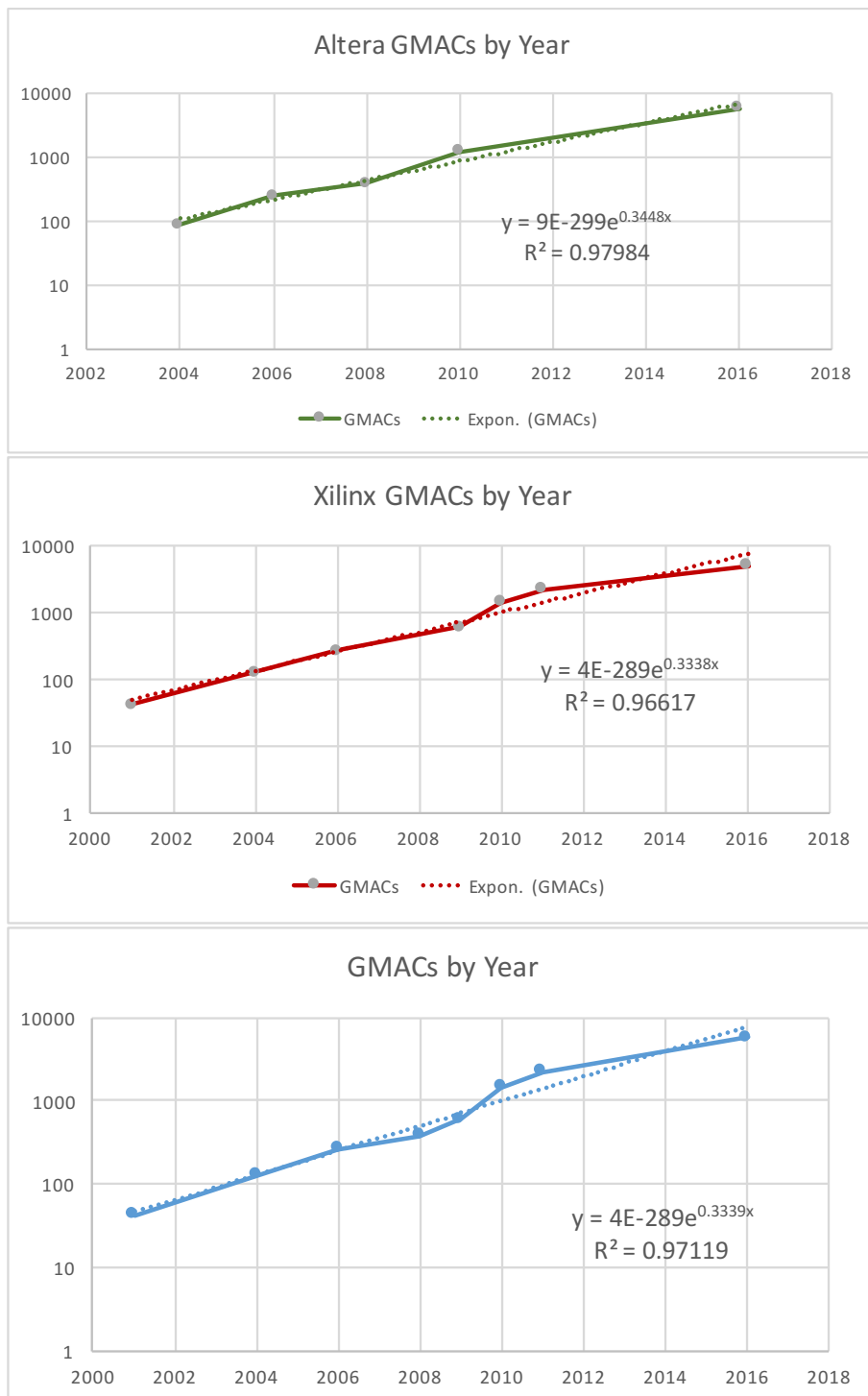


Figure 48: Progress of FPGA processing power by year expressed in giga multiply-accumulates per second (GMACs). Both Xilinx and Altera are increasing their max DSP processing power by about 40% per year (top plots). The bottom plot shows the best result over both Xilinx and Altera.

8.7 Frequency processing trade off

In connection to an FFX correlator, the first coarse F channelization may happen at the ALMA antenna, or at the main correlator location. Both options are technically possible but have pro's and con's demonstrated by the following table 22. Clear preference for first coarse F location at the antenna can be demonstrated by much lower transport bandwidth required.

Type	Power	Transport Bandwidth	Calculating power	Upgrade/Update
at antenna	medium	4x16 Gbps	High	easy
at correlator	medium	8x16 Gbps	High	easy

Table 22: Calculation engine trade-off

8.8 Cost estimates

In this section cost estimation will be done for proposed alternative configuration of digital front-end that provide technical solution which fulfills main specifications and function requirement outlined in this document. We will consider main digitization options as well as some analogue modifications of current ALMA signal chain design which would be needed to tighten the analogue dynamic range which is required by several digitization solutions.

8.8.1 Wide band digitizer option.

For the wide band down converter option the main cost driver is cost of very high speed ADC. We consider here that ADC can digitize the entire IF band 4-18 GHz and the analogue down conversion is not needed. As result we have the simplest analogue part among all considered options. It consists of a wideband high power variable gain amplifier and a Nyquist band filter. Cost estimate for major components is reflected in table 23.

Table 23: Cost table for Wide band down converter option for one analogue channel.

Item	Value	Comment
Input power amplifier	\$300	Input amplifier 0-20 GHz
Nyquist filter	\$20	Directly in PCB - 9 pol
ADC-1	\$6000	ADC from the table 18
PCB	\$100	PCB board manufacturing/per board
Total	\$6420	Total assuming negotiated ADC prices

The total cost of this digital front end solution per antenna will be $\$26000 + \$7000 + \$1000 = \34000 , assuming full production. This number includes the cost of DSP which is discussed in detail in section 8.6. We adopt the current price of DSP here, but will consider a price projection for 10 years in the trade of section. Another contribution to total cost per a antenna is cost of digital transfer high speed TCP/IP connection and control computer components.

8.8.2 High dynamic range down converter/digitizer combination option.

When containerized components are used to build up scheme like in figure 45 in the section section 5.4 price of analogue components of single down converter module can be substantial. Typical cost of an amplifier module is of order of 300..500 Euro and LO module is of order of few thousands Euro. However, prices of equivalent surface mounted components are substantially smaller, reaching level of 10..20 Euro per functional chip. Prices will go further down for components within 0-30 GHz range due to high demand in high speed digital fiber optical data link solutions as well as the advent of 5G cellular network hardware. With proper designed high frequency PCB, including printed directional couplers and RF filters, associated cost of analogue components can reach small fraction of the ADC chip cost. Similar benefit applies to synthesizers on chip modules (as example from Analog Devices). We consider a practical example of what can be achieved using state of the art COTS components as of year 2019 in the table 24.

Table 24: Example of current (mid 2019) COTS components list for a basic down converter module with 5 GHz processing bandwidth. Based on analog.com website information

Item	Value	Comment
Input amplifier	\$70	Input amplifier 0-20 GHz
Baseband amplifier	\$110	0..6 GHz amplifier
Double Balanced Mixer	\$22	RF/LO 3-20 GHz, IF 0-6 GHz
Input filter	\$20	Directly in PCB 7 pol
Nyquist filter	\$20	Directly in PCB - 9 pol
LO synthesizer - 1	\$71	LO synthesizer chip 62 MHz..16 GHz
LO synthesizer - 2	\$275	LO synthesizer chip 62 MHz..32 GHz
ADC-1	\$3100	AD9213 10.25 GSPS/12 Bit
ADC-2	\$2000	AD9213 6.25 GSPS/12 Bit
PCB	\$100	PCB board manufacturing/per board
PLL components	200	PLL components for high quality phase lock loop
total	\$ 6000	Total including LO synthesizer 1 and ADC-1 option

Components listed in the table are surface mounted component which can be placed on a high frequency printed circuit board (PCB). PCB manufacturing costs are included. We do mention two types of LO synthesizers, the minimum required and a very wide band (0.063-32 GHz) versions. For calculating estimate price per down converter channel we use minimum required LO chip costs referred as LO synthesizer 2 in the table. As available now cost estimate per down converter channel based on 10.25 GSPS 12 bit ADC is **\$3700**. While it is reasonable to assume that a lower 8 ENOB ADC type would cost much less but still be sufficient, we can use ADC cost as \$2000 per unit and arrive to cost of **\$2600** per down-converter module sub-band. In total these estimates evaluate to **\$15000** and **\$10500** respectively per 4 module 2-19 GHz wide down converter, see frequency plan in figure 44. It is expected, that digitization speed in terms of GSPS will be pushed slightly up in the future with price only going down, while less down converter modules will be required to cover the same bandwidth. Another compromise can be made, considering, that first band in figure 44 top needs ADC of half the speed of the main ADC.

Current and future ALMA configuration requires simultaneous digitization of four analogue outputs. This brings us to down converter + ADC price range of **\$50000...68000** per antenna which includes processor FPGA which will be similar for full band ADC and for downconverter modules and costs additionally **8000\$** see the previous section for DSP. A 12 ENOBs corresponds to instantaneous dynamic range of 72 dB. With this dynamic range the digital front-end system can calibrate out IF pass band ripple of >20 dB while still capable of doing full digital Hot/Cold/Sky signal power leveling and sending full 4 bit to correlator. Specifications on any analogue parts of the system can be significantly relaxed, design simplified and cheaper components can be used for down converter modules. High dynamic range also allows the digital system to tolerate higher level of spurious signals without deterioration of system performance.

8.8.3 High dynamic range down converter, RFSoc option.

As discussed in section 5.3.6 utilizing highly integrated RFSoc option may prove to provide significant system advantages but also very large costs benefit. We estimate cost of this option in the following table 25.

The total price of the components per one analogue channel is **\$1632 x 4 = \$6538** and correspondingly price of this option per antenna is **\$6538 x 4 = \$24122**. The price per antenna already includes the necessary DSP and the data transfer which is already integrated into the RFSoc chip. This number is already lower than the cheapest digitization at once option showing the power of integration. This number does not change significantly if 8 analogue channels will need to be used per RFSoc because RFSoc chip clearly dominates the cost.

Table 25: Estimate of costs of components for RFSoc solution based on XILINX RF soc as of 2020, per frequency subbands. Assuming 4 analogue subbands are needed to cover 20 GHz bandwidth

Item	Value	Comment
Input amplifier	\$70	Input amplifier 0-20 GHz
Baseband amplifier	\$110	0..6 GHz amplifier
Double Balanced Mixer	\$22	RF/LO 3-20 GHz, IF 0-6 GHz
Input filter	\$20	Directly in PCB 7 pol
Nyquist filter	\$20	Directly in PCB - 9 pol
LO synthesizer - 1	\$20	Only VCO is needed
RFSoc	\$5000	Based on xilinx demo board price of \$9000
PCB	\$100	PCB board manufacturing/per board
PLL components	20	PLL components for high quality phase lock loop
total	\$ 1632	Total including quarter of RFSoc cost

8.8.4 Analogue modifications cost analysis

Absolute cost estimate of analogue part of front end which includes front end cartridge is not part of this study. It should also be recognized that the receiver costs for different RF bands can be significantly different. For digital front end study it is however needed to estimate relative costs of low ripple/slope highly integrated option v.s. a high bandwidth option which we consider to have the same costs as current ALMA bands because technology has advanced since first version of ALMA has been built. In the following table we will estimate additional costs due to the tighter dynamic range specifications for digitization at once option. We will use the following approach, we will consider model signal chain costs and produce differential costs estimate for the low pass band ripple and the standard pass band ripple option. Table 26 summarizes the estimated costs per each element of one signal chain which corresponds to one polarization channel of ALMA cartridge and includes double IF signal chain. The low ripple option cost estimate column in the table is differential increase of cost due to tightening the ripple specifications.

Table 26: Example of current (mid 2019) for basic one polarization signal chain. Differential cost increase show in the third column for the low ripple signal chain option.

Item	Base cost	Low ripple Cost Increase	Comment
2SB SIS mixer	\$30000	\$10000	2SB mixer 1x
Isolator	\$12000	\$2000	Isolator 2x
IF hybrid	\$1000	\$500	Isolator 2x
Cryogenic IF amplifier	\$12000	\$4000	wideband If amplifier 2x
If cables	\$2000	\$500	IF cables inside cartridge 6x
Warm IF amplifiers	\$2400	\$400	Warm IF amplifiers x4
IF slope corrector	\$0	\$400	x2, only needed in one option
total	≈\$65400	≈\$17800	

As seen in the table, the total difference per single chain is \$17800 and per cartridge is **\$25600** which is approximately 27% of total cost of baseline cartridge chain which is a significant increase. The is also 46% of wide band digitizer cost per antenna just for one cartridge system. In principle all receiver cartridges must fulfill tighter ripple specifications in order to be able to operate with full bandwidth digitizer option. This means that calculating cost impact per antenna one should roughly multiply the cost difference per cartridge by 10 arriving to a **\$256000** cost per antenna. While the analogue modification costs are the least accurate among the estimates in this memo, the costs per antenna of trying to reduce system pass band ripple in an analogue way is still very significant.

8.8.5 Cost summary table and comparison

To provide very preliminary the costs estimate of different considered options we would like to present the summary table 27 outlining cost of different options per antenna as discussed in previous sections. From the price point of view, it is clear that any option requiring tightening of the passband ripple in an analogue domain has a negative impact on the component costs, which needs to be further clarified. This section is work in progress and is intended to underline possible issues in considering total costs of upgrade.

Table 27: Summary cost table for considered options.

Considered option	Cost per antenna	Analogue Modification Cost	Comment
Wide band digitizer	34 k\$	up to 26 k\$* per cartridge (TBC)	low pass band ripple required
Discrete down conwerter	\$50..68 k\$	0	
RFSoc downconverter	\$25 k\$	0	Highly integrated

* This costs is only required if full bandwidth digitization would not demonstrate sufficient dynamic range. For the future development or upgrade, this cost can also be attributed to a cost of cartridge upgrade for an increased IF bandwidth which will be spread over many years.

9 Risk assessment

In this section we discuss risks associated with digital front end options as outlined in cost estimate section 8.8. These are just first considerations on risks and that not only cost estimates but also design maturity etc. need to be carefully addressed before an ADC solution is adopted.

9.0.1 Wide band digitizer option.

Main risks associated with wide digitization options are related to the very challenging very high speed ADC chips. The risk summary is presented in table 28

Table 28: Risk summary for digitization at once option.

Risk	Severity	Description
Design maturity	low	While high speed ADCs has been available for a while and significant progress has been made to test these, bandwidth requirements sets an additional challenge. At the moment a dual core Micram ADC is considered for implementation. These are in full production and can be considered mature. The highest speed performance of such a high speed dual core ADC has recently been demonstrated but further testing in the lab is required and potential problems in the interferometric mode still need to be studied.
Costs	High	High speed ADCs are made by small specialized company. There is limited market for these chips. This makes any costs estimates very inaccurate.
Availability	High	High speed ADCs are made by small specialized company. There is limited market for these chips.
Technical risk	Medium High	High speed ADCs are naturally much more sensitive to clock timing, jitters and shape. Multi core operation and calibration at high clock is also more challenging then at lower clock rate.
Reliability	Medium	While featuring relative low component counts which increases system reliability, the receiver chip is run at very high clock speeds which results in high power dissipation at the chip die. The latter may reduce reliability of the option for long duration use.

9.0.2 High dynamic range down converter/digitizer

For this option the main risks are in technical area, such as multi core operation and RF spurious signals. Risks are listed in the table 29

Table 29: Risk summary for high dynamic range digitizer in combination with analog down converter.

Risk	Severity	Description
Design maturity	Medium	The high dynamic range but lower clock speed ADCs are available as COTS items from large production companies. This type of ADCs will be used within 5G technology. Practically all of the considered ADCs are multiple core. Dual core ADCs has been used in an interferometer (SMA, NOEMA) but side effects of using multiple core ADCs with two LO synthesizers for interferometry needs to be further considered.

Table 29: Risk summary for high dynamic range digitizer in combination with analog down converter.

Risk	Severity	Description
Costs risk	Low	Design is based on components off the shelf (COTS) solution which is available now. Cost are only expected to be lower over time. There is a big investment in large consumer based application sector of these components such as 5G and fast internet.
Availability risk	Low	All components are COTS type and are produced by a large companies such as AD.
Technical risk	high	Lower speed ADC are reliable and can be reliably calibrated in multiple core use. The main technical challenge of this option is presence of many high power tones that are in the band of neighboring channels which makes spurious signal suppression/calibration challenging. This is compensated to some extent by a high dynamic range of digitization which allows for digital spurious signal suppression. Another challenge is PLL of LO synthesizer should have low enough phase noise to be able to operate within an interferometer. While at lower clock frequency, the higher ENOB adds more stringent requirements to the system's clock jitters and shape.
Reliability Risk	Medium	All components of the system are COTS type with large usage heritage and good industrial design. Large component counts of this solution does elevate the risk of failure during operation.

9.0.3 High dynamic range down converter/digitizer, RFSoc solution

For this option the main risks are also in technical area, such as multi core operation and RF spurious signals. Risks are listed in the table 30

Table 30: Risk summary for RFSoc system in combination with analog down converter option.

Risk	Severity	Description
Design maturity	High	5G technology, for which these system designed for required a lot of attention and can enjoy high initial investment into design. In addition system is of high level of integration which reduces the risk of incompatibility of building blocks. This makes design of the RFSoc system very mature. The mm wave 5G bands does imply using down converters at the large scale which makes this design more reliable and associated risk low. While low risk for 5G technology is implied this does not mean the system is automatically suitable for use in an interferometer and maturity risk is evaluated as high.
Costs risk	Low	Design is based on components off the shelf (COTS) solution which is available now. Cost are only expected to be lower over time. There is a big investment in large consumer based application sector of these components such as 5G and fast internet.
Availability risk	Low	All components are COTS type and are produced by a large companies such as Xilinx and have large consumer base such as 5G applications.

Table 30: Risk summary for RFSoc system in combination with analog down converter option.

Risk	Severity	Description
Technical risk	Medium	Lower speed ADC are reliable and can be reliably calibrated in multiple core use. The main technical challenge of this option is presence of many high power tones that are in the band of neighboring channels which makes spurious signal suppression/calibration challenging. This is compensated to some extent by a high dynamic range of digitization which allows for digital spurious signal suppression. Another challenge is PLL of LO synthesizer should have low enough phase noise to be able to operate within an interferometer.
Reliability Risk	Low	All components of the system are COTS type with large usage heritage and good industrial design. RFSoc integration reduces component count and offsets presence of many down converter channels.

9.0.4 Analogue low pass band ripple option

For this option the main risks are also in technical area, such as multi core operation and RF spurious signals. Risks are listed in the table 31.

Table 31: Risk summary for Analogue low pass band ripple option.

Risk	Severity	Description
Design maturity risk	Medium	Requirement of flat pass band requires low return loss of underlying components. While many components do exist, their design needs to be modified to reflect that. As it has been discussed in ripple mitigation option, critical components such as SIS mixer will have principle limitation to have low $ S_{22} $ at high end of the band. This will demand amplifier mixer integration to covert ripple to slope. While such integration has been demonstrated previously, it remains to be shown the low noise temperature of the system in combination with low ripple.
Costs risk	High	Requirements of the low return loss at components interfaces drastically reduces the components yields during production. This results in much more component throughput and testing effort both in industrial COTS setting and in custom made components such as SIS mixers. This makes costs less predictable and costs overruns more likely.
Availability risk	Medium	While most of analogue components are available, critical components such as low noise cryogenic LNAs and SIS mixers require significant development and are not performing to stringent return loss specifications at this date.
Technical risk	Medium	Main risk is in development of SIS mixers with low return loss at high IF frequencies. Similar challenge exists for IF amplifiers. Extremely large IF bandwidth and high IF frequency at upper band boundary produces additional challenge as fractional bandwidth becomes larger.
Reliability Risk	Low	When developed, all components utilize the same technology that has been used for many years before and demonstrated high reliability. The reducing ripple effort does reduce overall component count which improves overall reliability.

9.1 Risks summary

Table 32 summarises the risk assessment outlined in previous sections of this chapter. It can be clearly seen that RFSoc based down converter has the lowest amount of risks associated. The Full band digitization option has the highest risks on its own. It requires the analogue low pass-band ripple option also to be implemented which makes costs risks especially likely since both options have high risk score at costs risk.

Table 32: Risk summary for all considered options.

Risk	Full band digitization	High dynamic range down converter	RFSoc based down converter	analogue low pass-band ripple
Design maturity	Low	Medium	High	Medium
Costs risk	High	Low	Low	high
Availability risk	High	Low	Low	Medium
Technical risk	Medium High	High	Medium	Medium
Reliability Risk	Medium	Medium	Low	Low

10 Suggestions for future development

Based on the analysis within this document we think the following important development factors could be explored for further study to improve their technical readiness levels. We consider here technology a development roadmap which can help to achieve optimum solution for DFE and its utilization in ALMA system. We note, however, that several of the suggestions here require development that will likely put them on time scales longer than those appropriate for implementation in the ALMA 2030 development roadmap.

- **Development of SIS mixers covering large instantaneous bandwidth and low noise HEMT amplifiers covering large RF bandwidths.**

This involves development of new designs of SIS mixers and amplifiers optimized for large IF bandwidth while maintaining a low noise performance. Measures to improve matching between components in the signal chain and reducing component counts should be considered. Integrating more components such as mixer bias circuit and filters either within SIS mixer chip or within an IF amplifier should be demonstrated. Other basic measures such as integrating SIS mixer and IF amplifier physically close to each other and using an equalizer circuit should be considered to further reduce the system pass band ripple.

- **Development of spurious signal suppression in two core ADCs.**

Demonstration of dual station correlation performance of this aspect. This becomes more relevant as all proposed solutions satisfying required dynamic range are essentially dual core. It should be noted that both SMA and NOEMA interferometers are currently using a dual core ADC solution. An application of a true quad or more cores ADC lies beyond ALMA 2030 framework.

- **Development/monitoring development of high speed high resolution ADCs and performing detailed trade off study of implementation within the concept.**

This is already on-going activity which needs to be maintained until a solution for ALMA has been chosen. Detailed measurements of ADCs performance for high digitization rates needs to be performed for large sample of ADCs.

- **A full end-to-end demonstration of the future DFE concept.**

This development should involve building the laboratory prototype of DFE concept that involves the following functions implemented at the antenna station: first F engine implementation; pass band ripple equalization (phase and amplitude); digital signal power leveling; ADC and standard network protocol fiber optics data transfer . The next step of this development should be demonstration of DFE concept on the two stations of ALMA (or any suitable radio interferometer) including, full FFX performance with data transfer to main correlator location, utilizing spare fiber optics cables. This will also enable much better cost estimate of possible upgrade.

11 Conclusion

We have proposed a change in current ALMA system architecture to extend digital processing at the antenna to provide high calibration accuracy and more digital dynamic range. The new component digital front-end would replace ALMA digitizer and transport system. We have established specifications of such system, compatible with current ALMA interfaces and in line of requirements of ALMA development roadmap document with main requirement of 5.6 ENOBs dynamic range of digitizing system. We have evaluated the impact of DFE on to system performance as is and found that 20% (30% peak) system efficiency improvement is possible due to better sideband /bandpass calibration and additional 30% improvement will be possible for spectral line surveys due to optimal IF band coverage. 20% improvement in correlation efficiency is aided by DFE with optimal data rates towards main correlator. The system concept is also backwards compatible with the current ALMA XF correlator but will work especially efficient with FX correlator while performing part of its work load at the antenna. A rough trade-off analysis has preliminary demonstrated that full band digitizer or down converter modules both followed up by an FPGA processing board are solutions to be considered in time scale of 10 years, without clear preference between them. Proposed DFE system will have large positive impact in reaching ALMA science goals towards 2030 timescale.

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